# RAM-4

## FUNCTIONAL DESCRIPTION

The IMSAI RAM-4 board provides up to 4K bytes of static random access memory. Designed to utilize the Intel 2111 or 8111 chips, the RAM-4 board can be flexibly configured to contain up to 4K bytes in 256 byte increments. The board address can be switch-or jumper-selected to any 4K block of the computer's 64K memory space. Tri-state bus drivers and a fully-decoupled on-card voltage regulator provide plug-in compatibility with either the IMSAI 8080 or the Altair computer systems.

Either of the Intel 8111 or 2111 devices can be used on the RAM-4 board. The board has provisions for the use of standard as well as selected (high speed-450 n.s.) 8111 memories. Special circuitry allows extra delay time (1 extra cycle) for use by the slower memory. (Please consult the RAM-4 User's Guide for additional information about this feature.) The memory units provided by IMSAI with the RAM-4 board are 450 n.s. 8111's, requiring 0 wait cycles.

The RAM-4 also features write-protect, a capability useful in the development and debugging of programs. Four separate write-protect switches are provided on the RAM-4 board, each controlling a separate 1K of memory.

Physically, the RAM 4 board is G-10-equivalent, 1/16" glass fiber reinforced laminate. Plated through-holes eliminate jumpers, and the edge connector contact fingers are gold plate over nickel for reliable contact and long life. The board measures 5" x 10", and uses the standard 100 pin edge connectors (dual 50 pin on .125" centers) for electrical connections to the back plane. Discrete components are of the highest quality, with tantalum by-pass and ceramic de-coupling capacitors. The on-card regulator is protected against short circuits and thermal overload.

THEORY OF OPERATIONS

The RAM-4 board has space for 4K bytes of memory which consist of 32 chips of Intel 8111 or 2111 type random access memory organized 256 words x 4 bits wide in each chip.

These RAM devices are arranged on the board in a 2 x N (1≤N≤16) array, with the top row A containing bits 0, 1, 2, 3 of all the data and Row B containing bits 4, 5, 6,and 7 of all the data. Read/write and address control is provided by a support network of Gates (C8, C9, C13) and a Decoder (C10). Bi-directional tri-state bus drivers (C15, C16) are used to receive and transmit data to and from the IMSAI 8080 System bus.

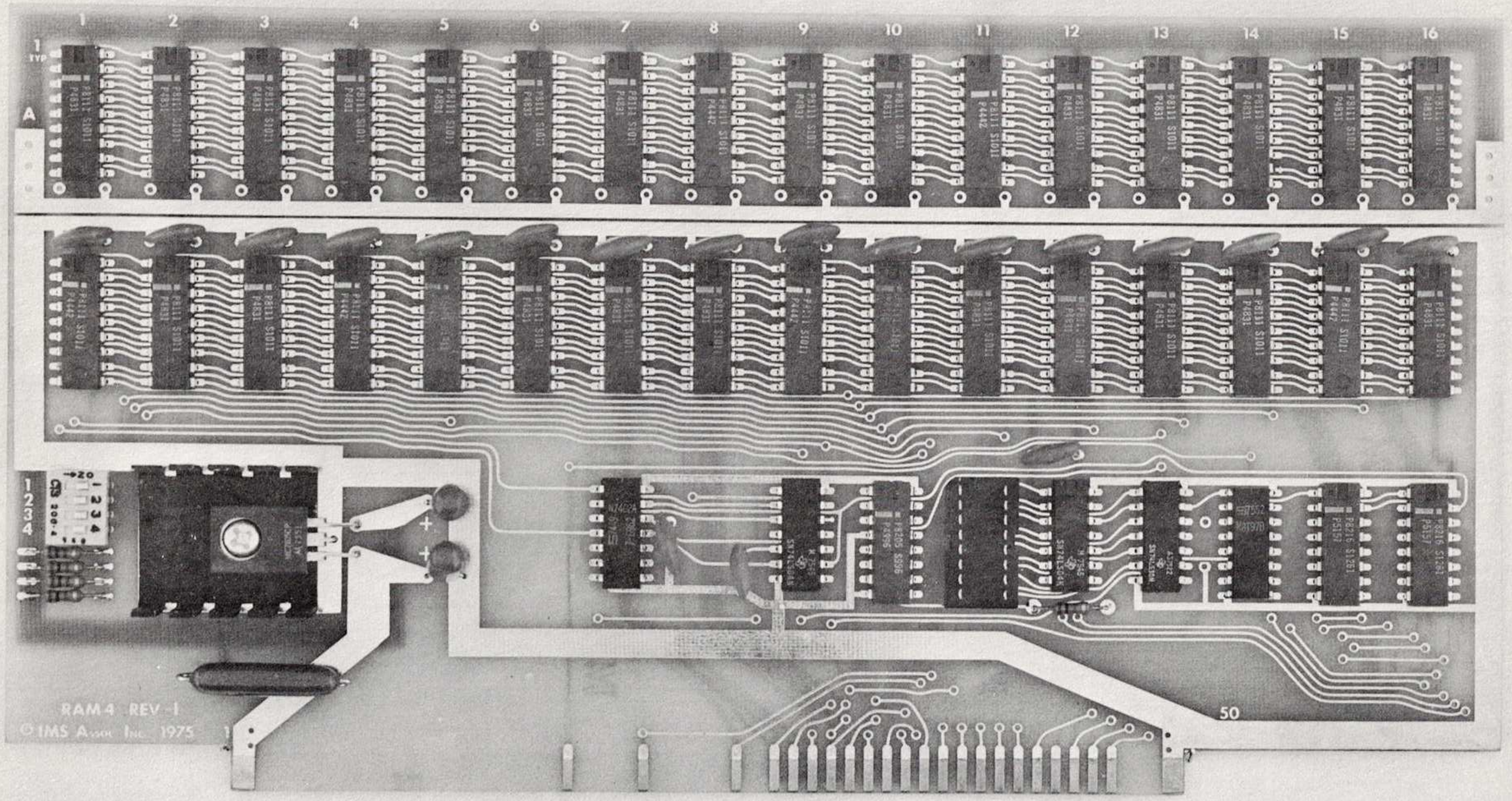
To begin the Read or Write Cycles, the board must be enabled. As shown in the schematic, the board enable is produced by an 8-input NAND (741s30 in position C13). Four ofthe NAND inputs are the jumper selected board address bits (A12, A13, A14, A15 or complements), and the remaining two are the inverted status bits SINP and SOUT. When the board is properly addressed, the NAND output is driven low. The 8205 1-of-8 decoder is then enabled, addressing a particular memory chip pair uniquely determined by the states of A8, A9, A10 and A11.

The 8T97 bus driver (C14) is also driven by the NAND (C13). When the input to the 8T97 is the signal, PWAIT, a cycle delay for the slower memory is produced by this buffered driver.* Also enabled at this time are the 8216, (C15, C16) tri-state bi-directional bus drivers.

The direction of data flow is determined bythe 7402 in position C8 which when low selects a data path going from the IMSAI 8080 data bus to the RAM-4 board's data bus. This is made low by either the memory write line from

*When sufficiently fast memory chips are used, the input to this gate should be connected to the tie 5 line so that the processor gets a ready signal immediately upon the board enable and does not wait one cycle. The tie 5 line appears on C10 Pin 6 and is simply a high logic level provided through the 1K resistor to +5 volts.

the control panel or the complement of the memory read status signal from the processor. Thus for normal operation, with the machine running, the status signal memory read determines whether these data bus drivers are driving to the IMSAI 8080 data-in bus or are receiving inputs from the IMSAI 8080 data-out bus. When the machine is stopped and the front panel is being used, the direction of data transmission is selected by the memory write pulse from the front panel. When writing from the front panel, a delay is necessary before turning off the data on the memory chips (so that there is time for the memory chips to write on the trailing edge of the write strobe before the data disappears) and this delay is provided by the disc capacitor to ground connected at the output of the inverter at C9 Pin 8. In addition to selecting the direction of data flow thru the bi-directional data bus drivers, the direction control signal is also inverted and applied to the output disable pin on the 8111's so that during writing the 8111 is receiving data on its bi-directional data pins and not attempting to drive. The write strobe is applied to the 8111's thru a 4 section data out DIP switch which enables the programmer to turn off the write pulse for each K for debugging purposes. When the machine is running normally, the write strobe comes from the processor write strobe line (pin 77 on the back plane) and when the front panel is being used, the write strobe line comes from the front panel on the memory write line (pin 68 on the back plane.) Two other sections of the 7402 are used to take either one of these write strobes and buffer them to drive the memory chips.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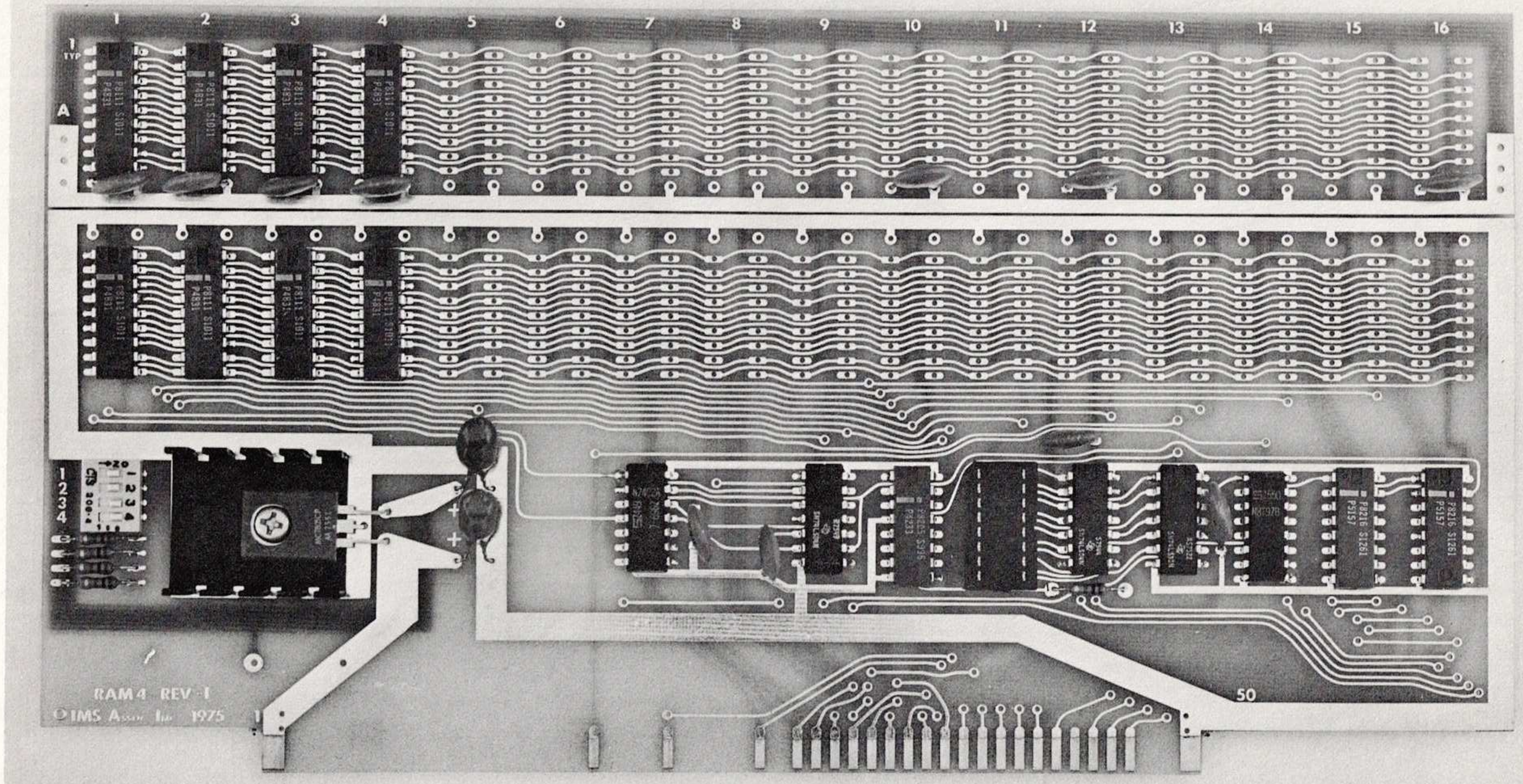
RAM 4-4 REV 1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**RAM 4-1 REV 1**

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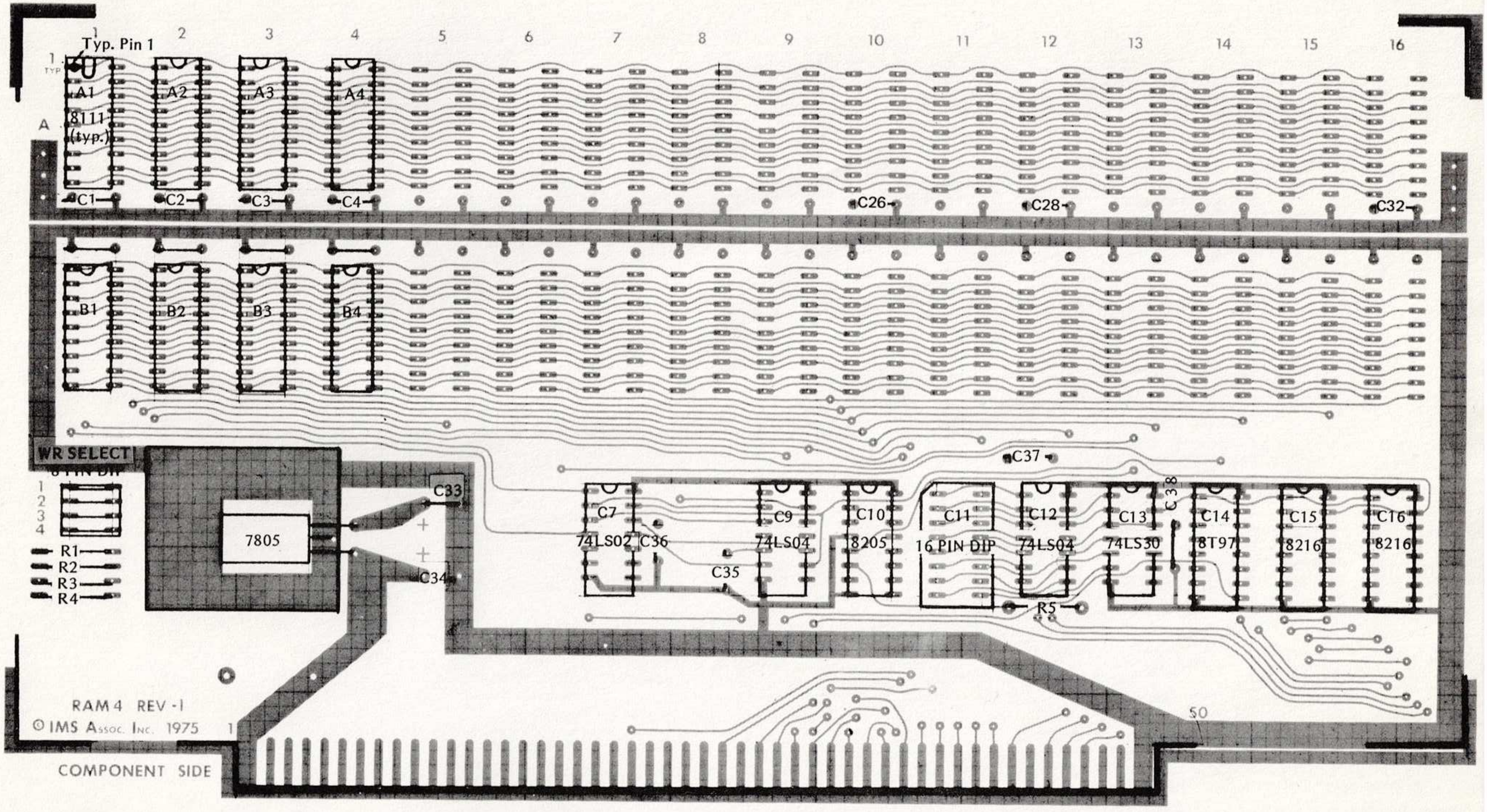


# IMS Associates Inc.

## ASSEMBLY DIAGRAM

## RAM 4 1K BOARD REV. 1 11/75

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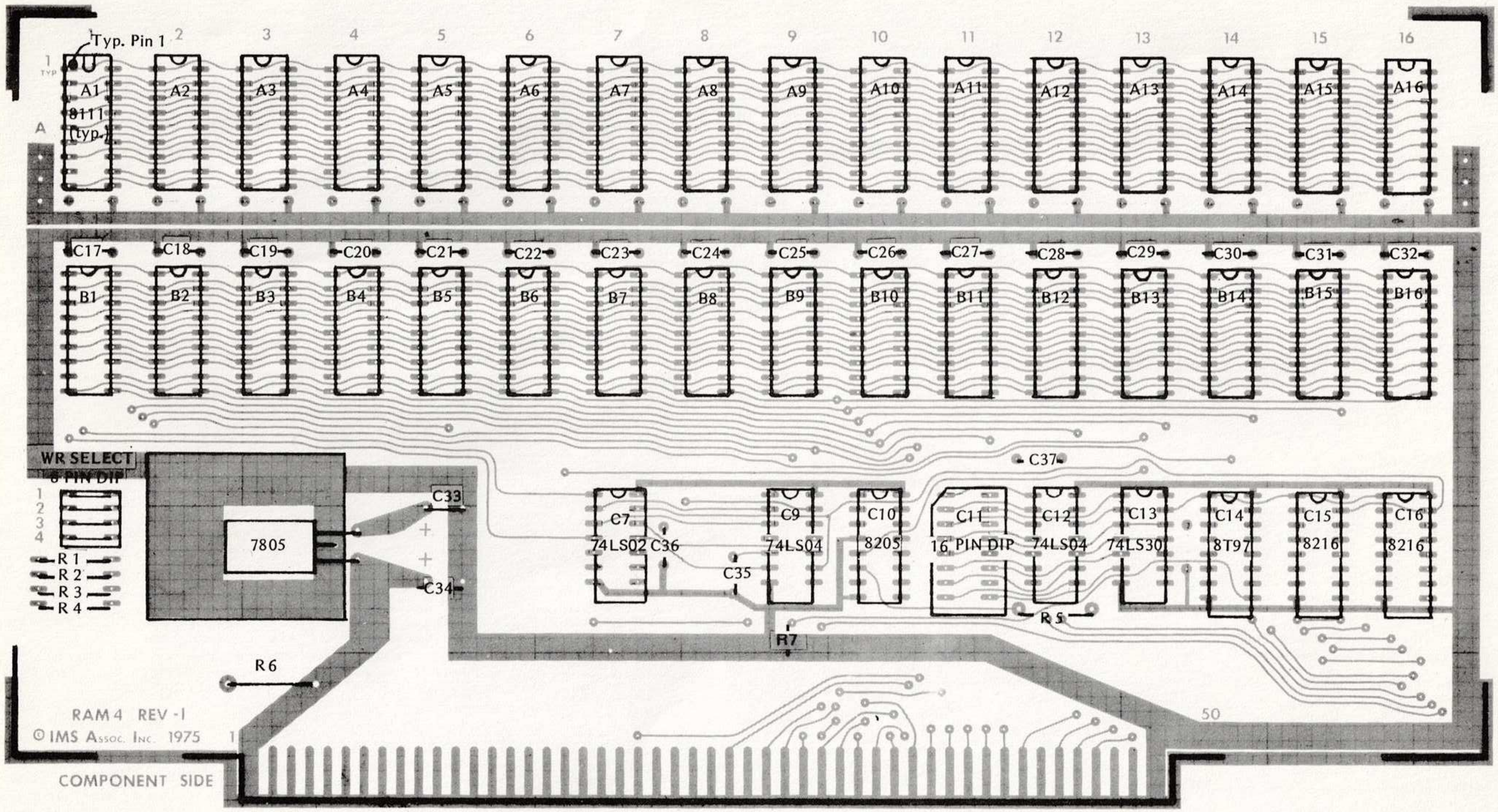



# IMS Associates Inc.

## ASSEMBLY DIAGRAM

RAM 4 4K BOARD REV.1 11/75

2/25/76

BOARD: RAM 4

| Part # | Quantity | Description | Identifying Marks |
|---|---|---|---|
| 74LS02 | 1 | Quad 2 Input NOR | SN74LS02N |
| 74ls04 | 2 | Hex Inverter (Low Power Schottky) | SN74LS04 |
| 74ls30 | 1 | 8 Input NAND (Low Power Schottky) | SN74LS30N |
| 7805 | 1 | 5 V. Positive Voltage Regulator | MC7805CP |
| 8111 | 8/1K | Static MOS RAM | P8111-2/S1013 |
| 8205 | 1 | High Speed Binary Decoder | P8205-S996 |
| 8216 | 2 | Bidirectional Bus Driver | D8216/S1261 |
| 8T97 | 1 | Hex Tri-State Buffer | N8T97B |
| dc-.1-30 | 4/K+3 | Disk Capacitor | 104Z/TDK |
| dc-.01-30 | 1 | Disk Capacitor | |
| h-hsto-220 | 1 | Heat Sink | Thermalloy/6106B-14 |
| h-pcs-d50-1/8 | 1 | 100 Pin Connector | CPH8100-100S+ |
| ich-16 | 1 | Integrated Circuit Header | Numbered 1-16 |
| pc-ram4 | 1 | Printed Circuit Board | RAM 4 REV -- |
| r-1K-¼ | 5 | 1K, ¼ Watt Resistor | br/bl/red/gold |
| s-ds-4pole | 1 | 4-position Dip Switch | |
| sts-16 | 1 | Solder Tail Socket | 16 Pin Socket |
| tc-33-25 | 2 | Tantalum Capacitor | 3325+2 |
| s/n/lw | 1 ea. | Screw/Nut/Lockwasher | |
| r-470-¼ | 1 | 470, ¼ watt resistor, yellow/violet/brown | |
| r-7.5-5 | 1 | 7.5ohm, 5 watt resistor (large) 4-4 Ram only | |
| solder | | | |

ASSEMBLY INSTRUCTIONS

Begin by bending the leads on the 5 1K ohm (brown, black, red) resistors. Install on the board and solder.

Next, install the eight integrated circuits on Row C. Check them for proper orientation (Pin 1 towards top of board) and/or bent pins, and carefully solder them to the board.

Install the 8111's in the desired locations (consult User's Guide), check orientation and pins, and solder.

Install .1 UF disc de-coupling capacitors (1 per 2 8111's) and solder.

Fasten the 7805 regulator and heat sink to the board with a #6 screw, lock washer, and nuts. Solder the 7805's pins in place. Install 2 .33 UF tantalum capacitors, (watch polarity, positive to positive) and solder.

Install and solder the .01 mf disc capacitor near C9.

Install and solder the 4 pole DIP switch and address socket or jumpers.

Visually inspect the board for solder splash or unsoldered pins.

USER GUIDE

The RAM-4 board uses Intel 8111 or 2111 memory chips which are organized 256 x 4 bits so that the minimum increment possible in the memory space is 256 x 8 x 8 bits or an increment of 256 bytes which consists of 2 memory chips.

The board is organized so that the appropriate low and high order bits are always in the same column. The positions are arranged in ascending order according to address, starting from column 1 thru column 16. Thus, while a 4K board has column 1 thru 16 all full, a 2K board which uses the lower 2K of the 4K memory space, would have columns 1 through 8 filled and a 1K board that uses the lower 1K of the memory space in the 4K board would have column 1 thru 4 filled.

It should be remembered that each position (A1-16, B1-16) represents a unique address, and that Row A contains bits 0-3 of all data, while Row B contains bits 4-7 of all data. Thus, the user has several options as to the possible structure of his memory space. For example, if a user desired a 512 byte memory, and, additionally, wanted those 512 bytes in the lower half of the 3rd K, he would place his memory chips in positions A9, A10, B9 and B10.

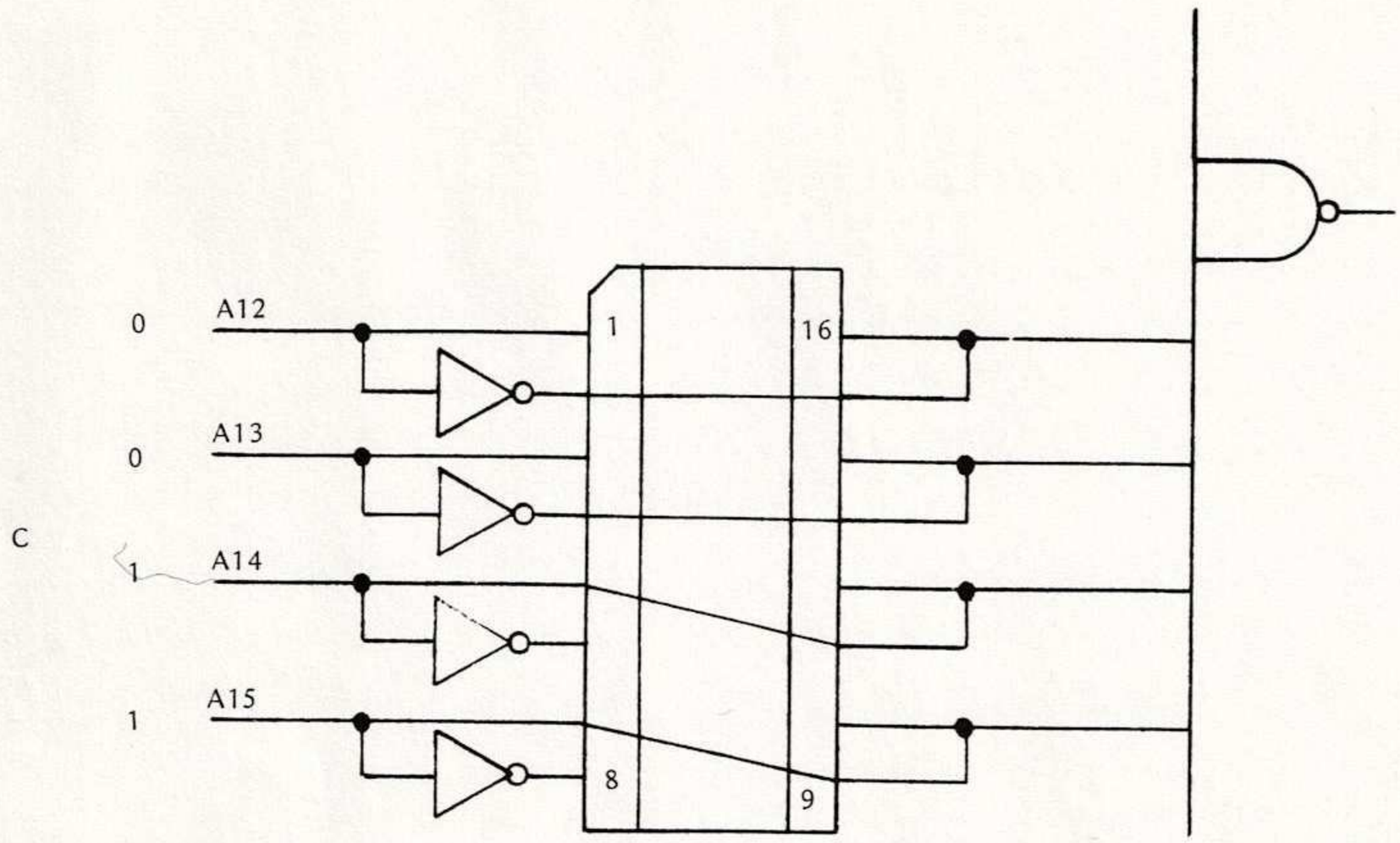
If in some column only one chip of the A-B pair is present, the appropriate position of the byte (A-0, 1, 2, 3, or B-4, 5, 6, 7) does exist in memory. The upper and lower byte portions are all independent, and the absence or presence of a chip in any position does not affect the operation of any other chip.

The 4 section write/protect switch is located between the power regulator heat sink and the left edge of the board. Each section of this switch affects 1K out of the 4K memory space on the board, and corresponds with the order of the memory chips on the board. That is, switch pole 1 controls writing in the lower 1K of the board, (columns 1 thru 4) and switch pole 2 controls writing in the second 1K block on the board, (columns 5 thru 8).

In order to write, these switches must be on. After a trial program has been written into memory, the appropriate switch may be placed off (without interrupting the power) and the program or panel will be unable to write into that block of memory. The data remains in memory, and reading from memory is not affected. This feature is very useful for debugging programs or when it is desired to run a program but eliminate any possiblity that mis-programming will cause any of the program to be over-written.

It is suggested that pins 9, 11, 13 and 15 be used to input as desired either a 0 or a 1 from the address bits so that for any address bits desired to be 0, the jumper will extend directly across the header and for any address bits desired to be 1, the jumper will extend diagonally across the header. For instance, if A15 were to be 1, the jumper would extend from pin 7 to pin 9. This makes it easy to visually tell what address the board is jumpered for.
An example jumper for the address block beginning with the address C hex is shown.

# BOARD ADDRESSING




The board address select jumper location is C11. It permits any one of the 16 possible 4K blocks of memory space to be jumpered to form the board enable.

The jumper location accepts a standard 16 pin IC socket and the jumpers can be soldered on to a header which can be plugged into the socket and changed easily without any resoldering from the board.

Address bits 12, 13, 14 and 15 are available on pins 1, 3, 5, and 7 and their respective complements on pins 2, 4, 6 and 8. These signals should be jumpered to the input of the board select circuitry which appears on pins 9 thru 16. An 8 position DIP switch similar to that used for write enable may be inserted into this location should very frequent changes of address be desired. For a board whose address is expected to remain the same, jumpers may be inserted directly on the board.