Industrial Micro Systems
IMS
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IMS-C00231 8K MEMORY BOARD

Your 8K STATIC RAM Memory Board (C00231) has been built and tested to industrial standards and can be expected to provide long, trouble free operation. The C00231 board is compatible with the S-100 Bus and will work with Altair, IMSAI, and other 8080 or Z80 computers using the S-100 Bus.

Memory "Strapping" is done by plugging the 2 position shunt on the appropriate pins of the address selection header.

Shunt Position	Address Range	(Hexidecimal)
0	0 to 8K	0000 to 1FFF
1	8 to 16K	2000 to 3FFF
2	16 to 24K	4000 to 5FFF
3	24 to 32K	6000 to 7FFF
4	32 to 40K	8000 to 9FFF
5	40 to 48K	A000 to BFFF
6	48 to 56K	C000 to DFFF
7	56 to 64K	E000 to FFFF

The C00231 Board has a "Phantom Line" incorporated in the logic for compatability with computers using this feature. (Processor Technology). The "Phantom Line" disables the memory board whenever it is at a logic low. A two pin header with shunt is provided for enabling the "Phantom Line" feature. If the "Phantom Line" is not used, it is recommended that the shunt be removed, disabling this logic. (Pin 67 of the S100 bus is used for the "Phantom Line".) We suggest storing the shunt on two unused pins of the address selection header if you do not use the Phantom Line feature. The pins on the numbered side of the address selection are all common and the shunt may be placed on any two of these pins.

The memory matrix as shown on page 2 of the schematic is in a one to one relationship with the physical board. Each row of 8 IC's services one bit of all addresses on the board. Bit identification is shown on the board as DØ0 through DØ7. The columns labeled CE0 through CE7 correspond to the individual 1K increments of the 8K memory. CE0 is the first K Bytes, CE1 is the second K Bytes, and so on through CE7.

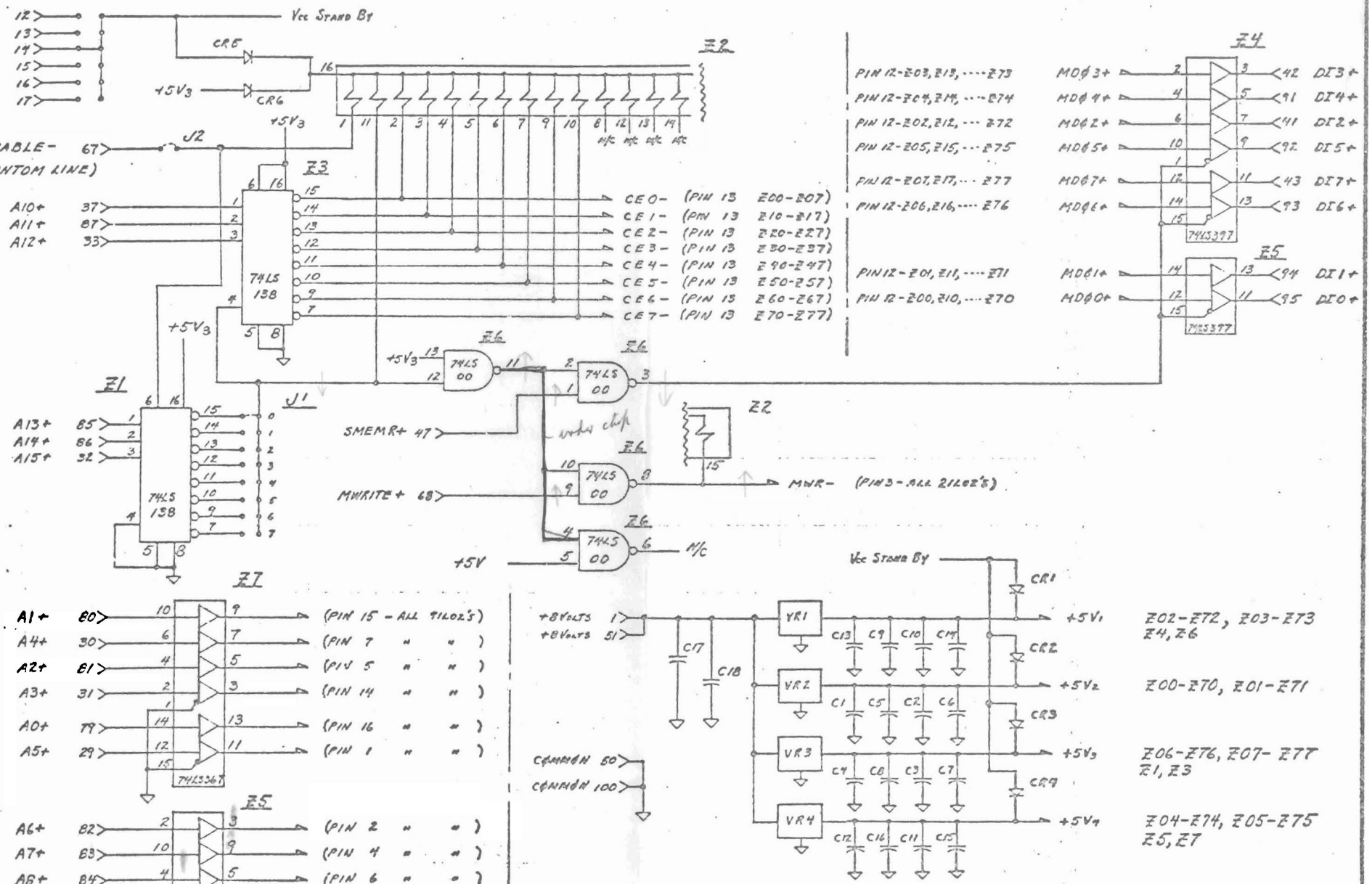
Address lines A13+, A14+, A15+ are decoded by IC Z1 and applied to the address strapping jack, J1. When A13+, A14+, A15+ decode to the address selected by the shunt, IC Z3 is enabled and decodes address lines A10+, A11+, A12+ selecting the particular 1K memory increment on the board. During a READ operation, the SMEMR+ signal from the processor enables the bus drivers to gate the memory data onto the the data bus. During a WRITE operation, the MWRITE+ signal from the processor causes data to be written into the selected memory IC's. The DISABLE- line (pin 67) disables IC Z1 when it is at a logic low thereby deselecting the memory board.

The IC sockets used on this board were chosen for their ability to provide a true gas tight joint necessary for long term reliability. The beryllium copper contact material in these sockets will not weaken with age and is superior to the normally used phosphur bronze material. The high contact pressure in these sockets makes IC removal slightly more difficult than some of the lower contact pressure sockets which cannot provide a true gas tight joint. Care should be taken when removing an IC from its socket not to bend the leads. Use either a "Chip-Clip" or a small soldering aid of screwdriver to carefully pry them out. Removal by fingers -- Ouch!

The power distribution on the board has been laid out to "share the load" during operation. During any Read or Write operation, two (2) enabled memory IC's are on each of the four regulators. In a similar manner, the decoupling capacitors also share the load.

The gold contact material on the edge connector is plated over a nickel base to prevent "copper migration" which occurs when gold is plated directly over copper. Copper molecules which reach the surface will oxidize and cause a large increase in contact resistance after an extended period of time. The underplating with nickel prevents this problem from occurring. Contact lubricants are not recommended and shouldn't be used.

As a word of caution, please remove power from your system when plugging or unplugging boards. Many IC's are destroyed by not following this simple rule and occasionally catastrophic failures occur. Nuff Said!



INDUSTRIAL MICRO SYSTEMS

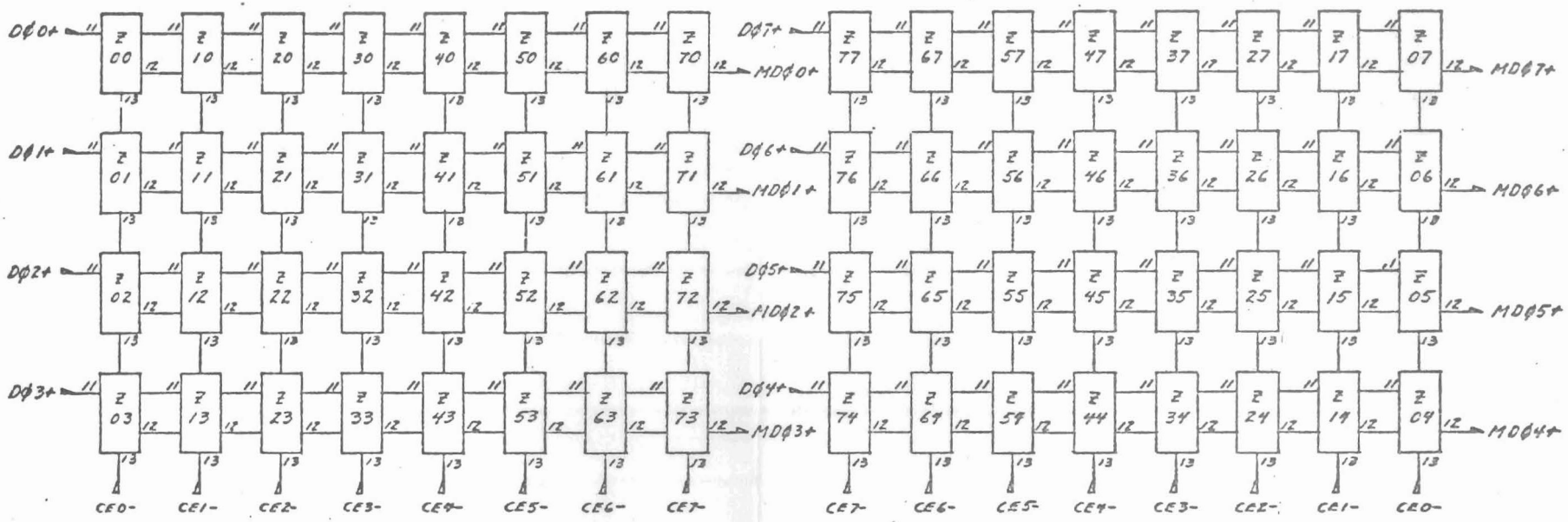
SCALE:	APPROVED BY:	DRAWN BY D.A.L.
DATE: 4-29-77	4-29-77	REVISED

8K STATIC MEMORY

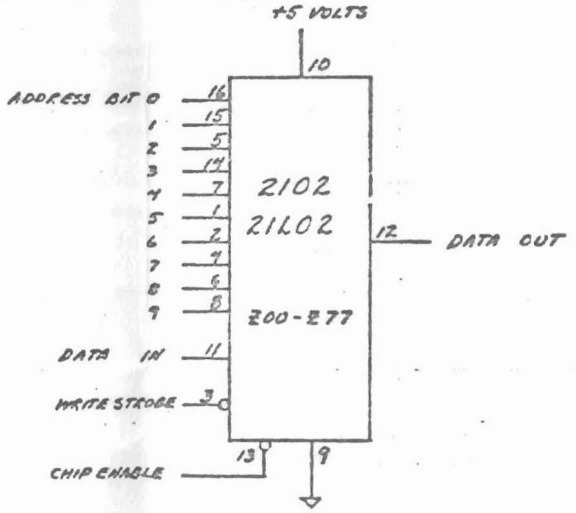
L00231

DRAWING NUMBER 1 OF 2

TOP OF BOARD



IDENTIFICATION	PART TYPE & NUMBER
CR1 THRU CR6	DIODE, IN4001
C1, C4, C5, C8 C9, C12, C13, C16	CAPACITOR, 6.8 mfd, 20V
C2, C3, C6, C7 C10, C11, C14, C15	CAPACITOR, .01 mfd, 50V
C17, C18	CAPACITOR, 15 mfd, 20V.
VR1, VR2, VR3, VR4	VOLTAGE REGULATOR, 5VOLT, LM340T-5
Z1, Z3	INT. CIRCUIT, 74LS138
Z2	RESISTOR ARRAY, 15 x 4.7K OHM
Z4, Z5, Z7	INT. CIRCUIT, 74LS367 (8T97 OR 74367 OPTIONAL)
Z6	INT. CIRCUIT, 74LS00
J1	JACK, DUAL 8 POSITION WITH SHUNT
J2	JACK, DUAL 1 POSITION WITH SHUNT



TYPICAL MEMORY IC

PIN 11	Z00-Z70	<36	DØ 0+
"	Z01-Z71	<35	DØ 1+
"	Z02-Z72	<88	DØ 2+
"	Z03-Z73	<89	DØ 3+
"	Z04-Z74	<38	DØ 4+
"	Z05-Z75	<39	DØ 5+
"	Z06-Z76	<40	DØ 6+
"	Z07-Z77	<90	DØ 7+

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SCALE:
DATE: 4-29-77
APPROVED BY: H.A.L. 4-29-77
DRAWN BY: DAL
REVISED:

8K STATIC MEMORY

100231

DRAWING NUMBER 2 OF 2