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HRAM
HORIZON Random Access Memory
USER / TECHNICAL MANUAL

00406B

CONTENTS

APPENDICES

This manual supplies the user of the HORIZON Random Access Memory (HRAM) board with information he or she needs to install the board and put it into operation. This includes information on selecting the various memory options, testing the board and resolving any difficulties associated with system integration.

The manual also provides information for service technicians and engineers who may wish to evaluate the technical aspects of the board or to undertake its repair.

1.1 GENERAL DESCRIPTION

The HRAM board is a random access memory board designed for use in the HORIZON computer system.

There are three versions of the HRAM board: HRAM-64 with 64K bytes, HRAM-48 with 48K bytes, and HRAM-32 with 32K bytes. The only significant difference between these boards is the amount of memory they contain. All three versions incorporate parity error checking and bank switching capabilities.

1.2 WARRANTY

North Star Computers, Inc., warrants the electrical and mechanical parts and workmanship of this product to be free of defects for a period of 90 days from date of purchase. If such defects occur, North Star Computers, Inc. will repair the defect at no cost to the purchaser. This warranty does not extend to defects resulting from improper use or assembly by purchaser, nor does it cover transportation to the factory. Also, the warranty is invalid if all instructions included in the accompanying documentation are not carefully followed.

Should a unit returned for warranty repair be deemed by North Star Computers, Inc. to be defective due to purchaser's action, then a repair charge (not to exceed $50 without purchaser's consent) will be assessed. ANY UNIT(S) OR PART(S) RETURNED FOR WARRANTY REPAIR MUST BE ACCOMPANIED BY A DATED COPY OF THE ORIGINAL SALES RECEIPT. The item should be returned to the dealer from whom the product was purchased, for implementation of the warranty. When sending the item to the factory for repair, the dealer must call the North Star Technical Hotline to receive a Return Material Authorization (RMA) number to accompany the item to the factory.

The following warranty limitation applies to units located outside the United States of America: All costs and arrangements for transportation of the product to and from the factory are borne entirely by the customer.

No warranty, expressed or implied, is extended concerning completeness, correctness, or suitability of the North Star equipment for any particular application. There are no warranties which extend beyond those expressly stated herein. This limited warranty is made in lieu of all other warranties, expressed or implied, and is limited to repair or replacement of the product.

1.3 SPECIFICATIONS

The HRAM specifications are given in Table 1-1.

Table 1-1

HRAM Specifications

Storage Capacity	32K bytes for the HRAM-32
	48K bytes for the HRAM-48
	64K bytes for the HRAM-64
Bits per Byte	Eight data bits and one parity bit.
Access Time	300 ns typical

CAUTION
The electronic components on the HRAM board may be damaged by the static electricity which often builds up in the human body. Before touching the HRAM board, discharge this electricity by touching a grounded metal object, such as the chassis of a Horizon which is plugged into the wall outlet. Follow this procedure each time the board is handled.

If the HRAM was packaged separately from the HORIZON, examine the contents of the carton to make sure they match the packing slip. Check to see if anything appears to be damaged due to shipping.

When handling the board, touch it only by the edges, to avoid contact with the sensitive components (see Figure 2-1). When laying the board down, place it on a flat surface with the components facing up.

Holding the HRAM

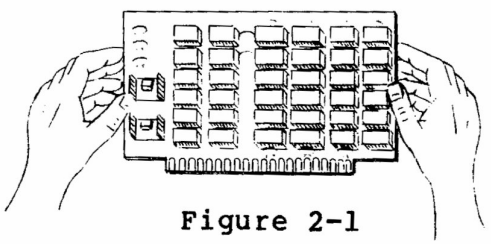


Figure 2-1

WARNING
DO NOT REMOVE THE COVER FROM THE HORIZON UNTIL THE POWER IS OFF, THE FAN HAS STOPPED, AND THE RED INDICATOR LIGHT ON THE FRONT PANEL HAS COMPLETELY DIMMED. DO NOT TURN THE POWER BACK ON UNTIL THE COVER HAS BEEN REPLACED.

2.1 INSTALLATION

To install the HRAM in the HORIZON, hold the memory board in one hand and touch the metal chassis of the HORIZON with the other hand as shown in Figure 2-2. This will eliminate any difference in static potential between the memory board and the computer.

Discharging Static Electricity

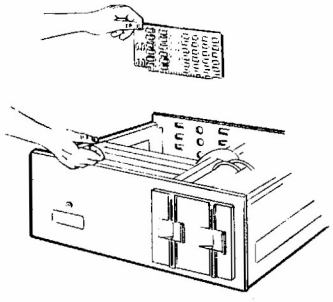


Figure 2-2

Hold the board by both edges, with the component side of the board toward the front of the computer. Slide the board into any empty slot in the HORIZON as shown in Figure 2-3.

Installing the HRAM

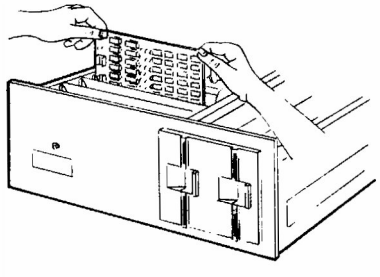


Figure 2-3

The row of metallic strips, or "fingers" on the bottom of the board should fit into the connector at the base of the card slot. Press firmly on the top of the memory board until the board is firmly seated in the connector.

2.2 REMOVAL

WARNING
NEVER REMOVE THE HRAM BOARD UNTIL THE POWER IS COMPLETELY OFF IN THE HORIZON.

To remove the HRAM, grasp the upper edge of the board. Avoid putting excessive pressure on the board components, and be careful of the sharp wire tips that project out of the back of the board. Pull the board out, and lay it down on a flat surface.

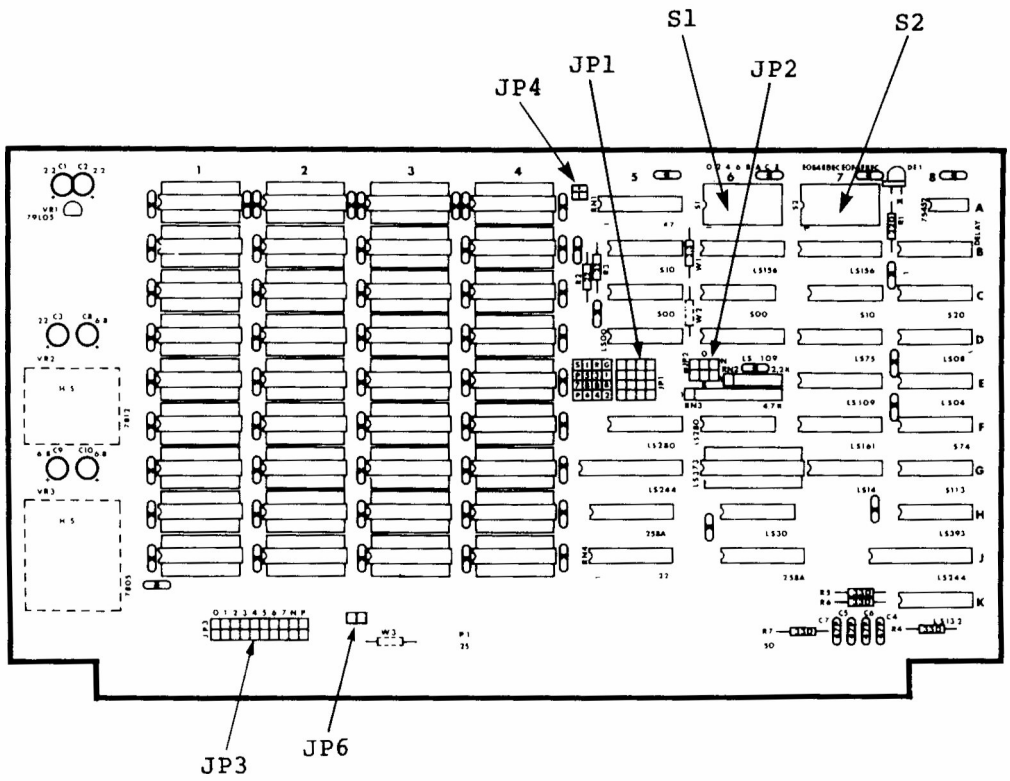
HRAM options are implemented by inserting and removing mini jumper plugs at various locations on the PC board and by changing the setting of the Memory Address switches. Figure 3-1 shows the locations of the jumper areas and the address switches on a 64K revision E board. Other boards differ as follows:

1. Jumper areas JP4 and JP6 do not exist on revision B boards.

2. Switch S2 is not installed on 48K revision B boards.

Instructions for determining the revision level of the HRAM board are given in Section 3.6.

Jumper Plug Areas and Memory Address Switches



Component	Use
S1, S2	- Select the active memory areas.
JP1	- Selects the bank status on reset and selects I/O control bits for bank switching and parity.
JP2	- Selects areas to be bank switched.
JP3	- Selects the parity error response.
JP4	- Implements the First Quadrant option.
JP6	- Reserved for future use. Do not install a jumper plug at this location.

Figure 3-1

The jumper areas consist of clusters of pins protruding from the PC board. When a jumper plug is plugged onto a a pair of adjacent pins, it connects the pins together. The jumper plugs are used to select various options on the HRAM Board as described in Sections 3.2, 3.4 and 3.5.

Each of the Memory Address switches, S1 and S2, is actually a group of eight switches in a single package. These switches are used as described in Section 3.3.

CAUTION
To reposition the jumper plugs, you must remove the HRAM from the HORIZON. Make sure the power is turned off and the red light on the front panel is completely out before you remove the HRAM.

To reconfigure the jumper plugs, lay the HRAM board down on a flat surface with the components facing up. You can move the jumper plugs with your fingers or a pair of long nose pliers.

3.1 EXAMPLE SYSTEM CONFIGURATIONS

This section shows the correct positions of the Memory Address switches and the jumper plugs for several example configurations of the HORIZON system.

3.1.1 EXAMPLE 1: THREE BANKS

In this example, the HORIZON contains three HRAM-64 Revision B boards, a standard Micro-Disk Controller board at E800H, and a Floating Point board at EFF0H. The switches and jumper plugs are shown in Figure 3-2.

On board 1, the memory between E000H through E7FFH and F000H through FFFFH is left on permanently, to contain the resident operating system. On the other two boards, the whole last 8K of address space (E000H through FFFFH) must be disabled, to prevent interference with the Micro-Disk Controller, the Floating Point board, and the 6K that contains the resident operating system.

In this case, the system contains three banks with the maximum 56K apiece and a resident operating system of 6K that is always left on. Each bank is switched off and on as a single unit. Bank 1 is configured to be turned on after the system is powered up or reset. Banks 2 and 3 are configured to be turned off after the system is powered up or reset.

Parity error checking is left in the standard North Star configuration.

Example 1

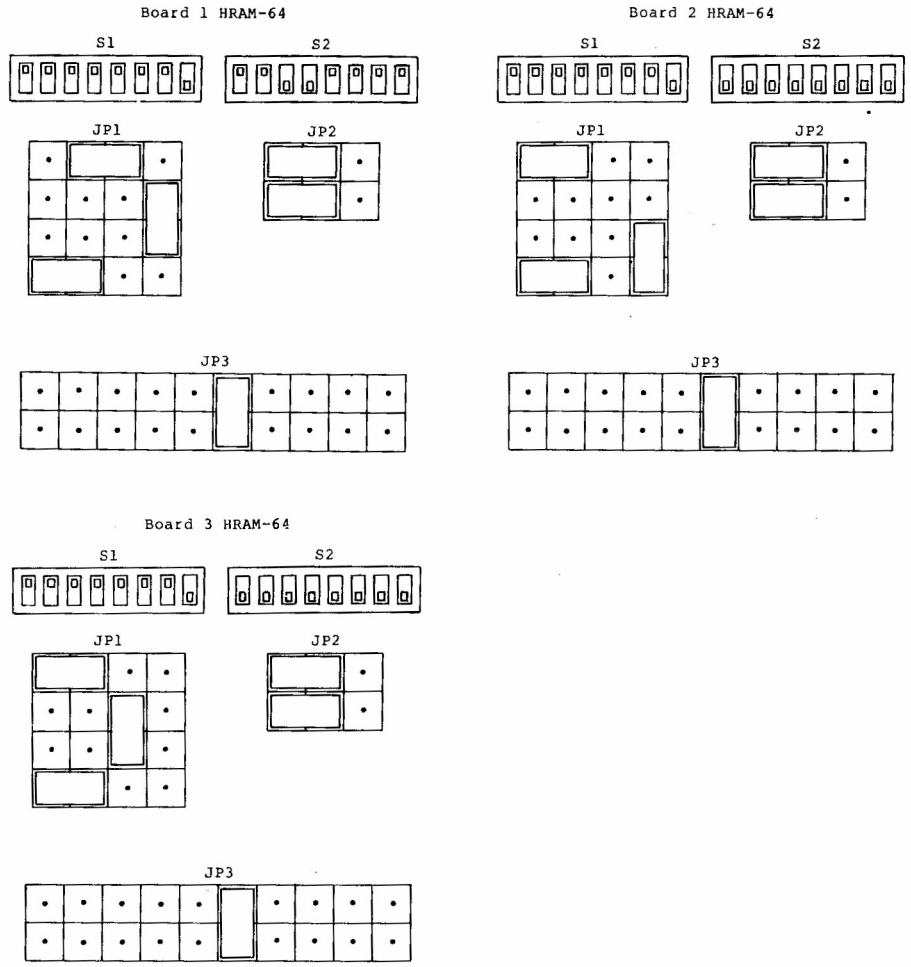


Figure 3-2

3.1.2 EXAMPLE 2: FOUR BANKS

In this example, the HORIZON contains one HRAM-48 board, three HRAM-32 boards, and a standard Micro-Disk Controller board at E800H. All HRAM boards are revision B. The switches and jumper plugs for this example are shown in Figure 3-3.

The 48K board is partitioned into two segments, 0000H through 7FFFH, and 8000H through BFFFH. An operating system that requires 16K of memory is loaded into the region between 8000H-BFFFH. This segment is always turned on. The other segment of this board is bank switched, and is designated the bank to be turned on when the system powers up or resets.

All three 32K boards have their memory starting at 0000H. All are bank switched off and on as single units, and all are programmed to be turned off when the system is powered up or reset.

Parity checking is left in the standard North Star configuration.

Example 2

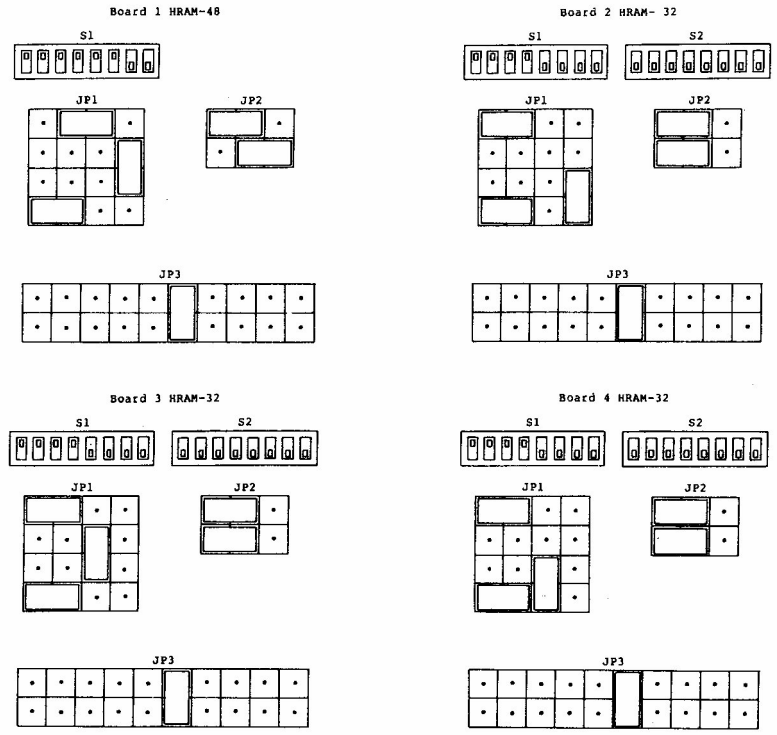


Figure 3-3

3.1.3 EXAMPLE 3: FOUR BANKS

In this example, the HORIZON contains one 32K HRAM board, three 48K HRAM boards and a standard Micro-Disk Controller at E800H. All HRAM boards are revision E. The switches and jumper plugs for this example are shown in Figure 3-4.

Only the lower half (0000H through 3FFFH) of the 32K board is used. An operating system is loaded into this half and it is always turned on.

All three 48K boards have their memory between 4000H and FFFFH, except for the 2K section E800H through EFFFH which must be disabled to prevent interference with the Micro-Disk Controller.

The three 48K boards constitute three banks which are switched as single units. One of these banks (board 2) is programmed to switch on when the system is powered up or reset, and the other two are programmed to switch off when the system is powered up or reset.

Parity checking is left in the standard North Star configuration.

Example 3

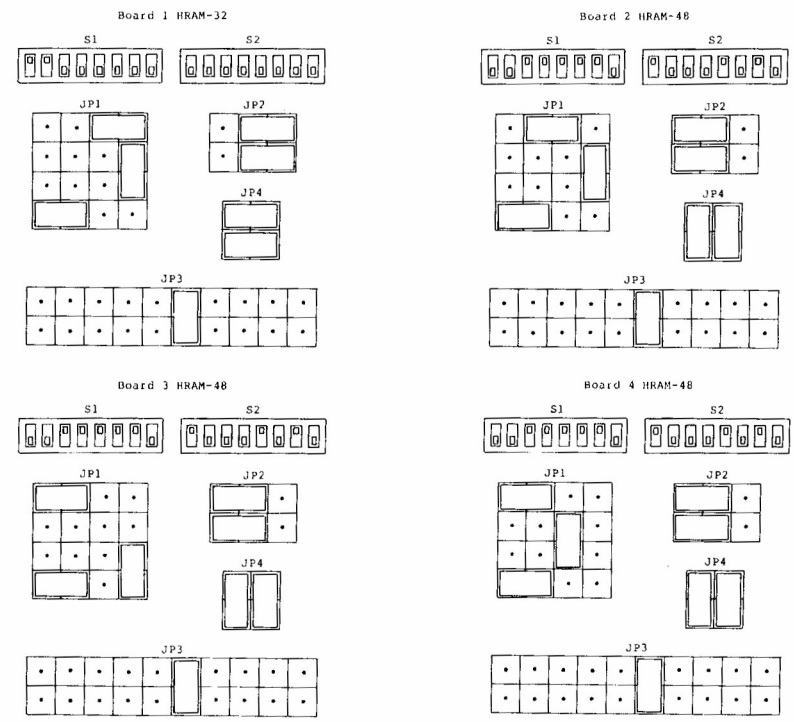


Figure 3-4

3.2 BANK SWITCHING

Bank switching is a capability that allows multiple memory boards to take turns using the same address region. Different memory "banks" are swapped in and out of the address region under software control, thus extending the HORIZON's memory capability beyond the limitation set by the processor's 16 address bits. This feature is particularly valuable in a multi-user environment, for it allows several users to share the same processor and operating system while maintaining different memory banks. Bank switching provides storage for a large array of data that will not fit into a single memory bank.

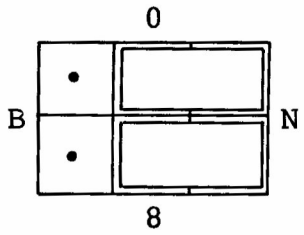
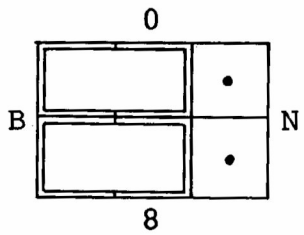
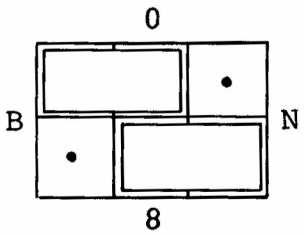
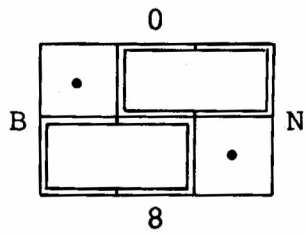
Only one bank at a time can respond to a specific memory reference. Such a bank is said to be "on". A bank is "off" when it does not respond to reads and writes from the processor. Although a bank that is off cannot accept data from, or provide data to the processor, the stored data continues to be refreshed, and remains intact.

3.2.1 Designating Switched Areas

For the purpose of bank switching, the HRAM board is logically divided into two 32K sections. The first section includes memory addresses 0000H through 7FFFH, and the second section includes addresses 8000H through FFFFH. Each of these sections may be bank switched when the board is switched on and off, or it may always remain on, depending upon the configuration of the jumper plugs as listed in Table 3-1.

Table 3-1

Bank Switching Configurations

Jumper Area JP2	Description
	Both halves of the board always on. Bank switching is disabled on this board.
	Both halves of the board bank switchable.
	The 32K section starting at 0000H is switchable. The 32K section starting at 8000H is always on.
	The 32K section starting at 8000H is switchable. The 32K section starting at 0000H is always on.

The last 8k portion of the HRAM board, E000H through FFFFH, may be enabled in a manner different than that described above, depending upon the setting of the Memory Address switches (see Section 3.3).

3.2.2 Designating I/O Port Control Bits

The user can choose any one of the six available I/O bits in Port C0H to control the switching of each bank. A jumper plug that connects any B pin in JP1 to any one of the adjacent pins, 1-7, allows the corresponding I/O bit to program the bank switching of this board (see Figure 3-5). With six I/O bits available*, it is possible to switch on and off a maximum of six memory banks. Figure 3-6 shows the position of the jumper plug on the HRAM board assigned to bank 3.

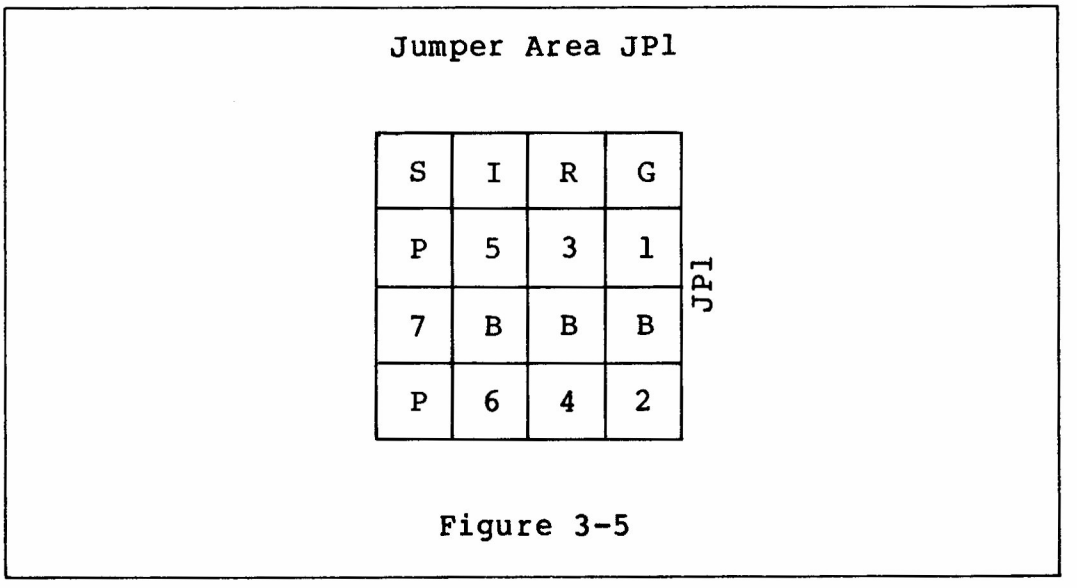


Figure 3-5

*One of bits 5, 6, or 7 is used for parity error control, leaving a total of six bits that can be used for bank switching. Note that bit 0 is used to control the on/off function specified by the other seven bits.

JP1 Set For Bank 3

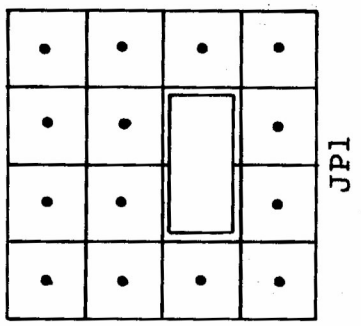


Figure 3-6

You must position the jumper-plug to designate a different bit on each board to be bank switched. If you want to combine two 32K HRAM boards into a single larger bank, program both boards with the same bit. A 64K cannot be divided into two different 32K banks.

It is possible to use earlier North Star RAM-32 or RAM-16 boards in conjunction with HRAM boards to create a bank switching system.

3.2.3 Software Instructions

The following instructions are an example of how to turn on or off memory bank 3. Memory bank 3 is composed of all those RAM boards that are configured to use I/O bit 3 for bank switching.

```
MVI A,08H    ; Turn on bank 3
OUT 0C0H

MVI A,09H    ; Turn off bank 3
OUT 0C0H
```

Note that bit 0 is used to specify turning the bank on or off. For different banks, change the program instructions accordingly. For example, to turn bank 5 on and off, the operands should be 20H and 21H instead of 08H and 09H.

Take care to allow only one bank to be on at a time. Section 3.2.4 describes the method for insuring that only one bank comes on when power is first turned on. When switching banks, the previous bank must be switched off before the next bank is switched on.

3.2.4 Bank Status on Reset

The HRAM is shipped with a jumper plug in the position shown in Figure 3-7. This connection causes the bank to always remain on.

JP1 Set for Bank Always On

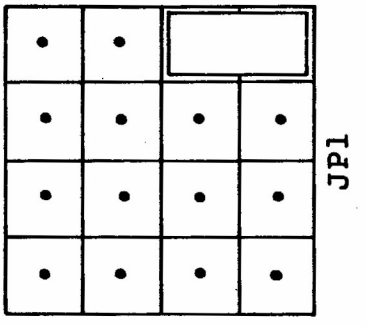


Figure 3-7

To enable bank switching, designate one bank as the bank to be turned on whenever the system is powered up or reset. On the board(s) that constitute that bank, move the jumper plug(s) to the position shown in Figure 3-8. This will cause all the memory in this bank to be on after the system is powered up or reset.

JP1 Set to Enable Bank on Reset

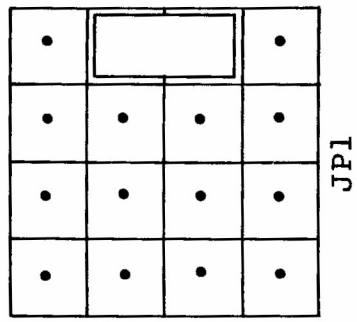


Figure 3-8

On the memory board for all other banks, move the corresponding jumper plug to the position shown in Figure 3-9. These banks will be turned off when the system is powered up or reset.

JP1 Set to Disable Bank on Reset

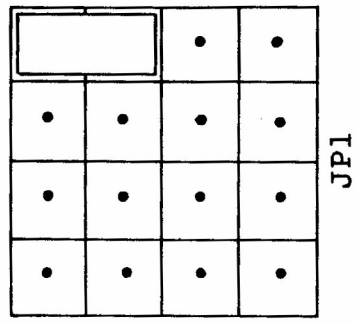


Figure 3-9

3.3 MEMORY ADDRESS SWITCHES

3.3.1 Revision B Board

The Memory Address switches allow the HRAM Board to respond to some sections of the memory address space and not to others. The correspondence between the Memory Address switches S1 and S2 on the revision B board and the address space is shown in Figure 3-10.

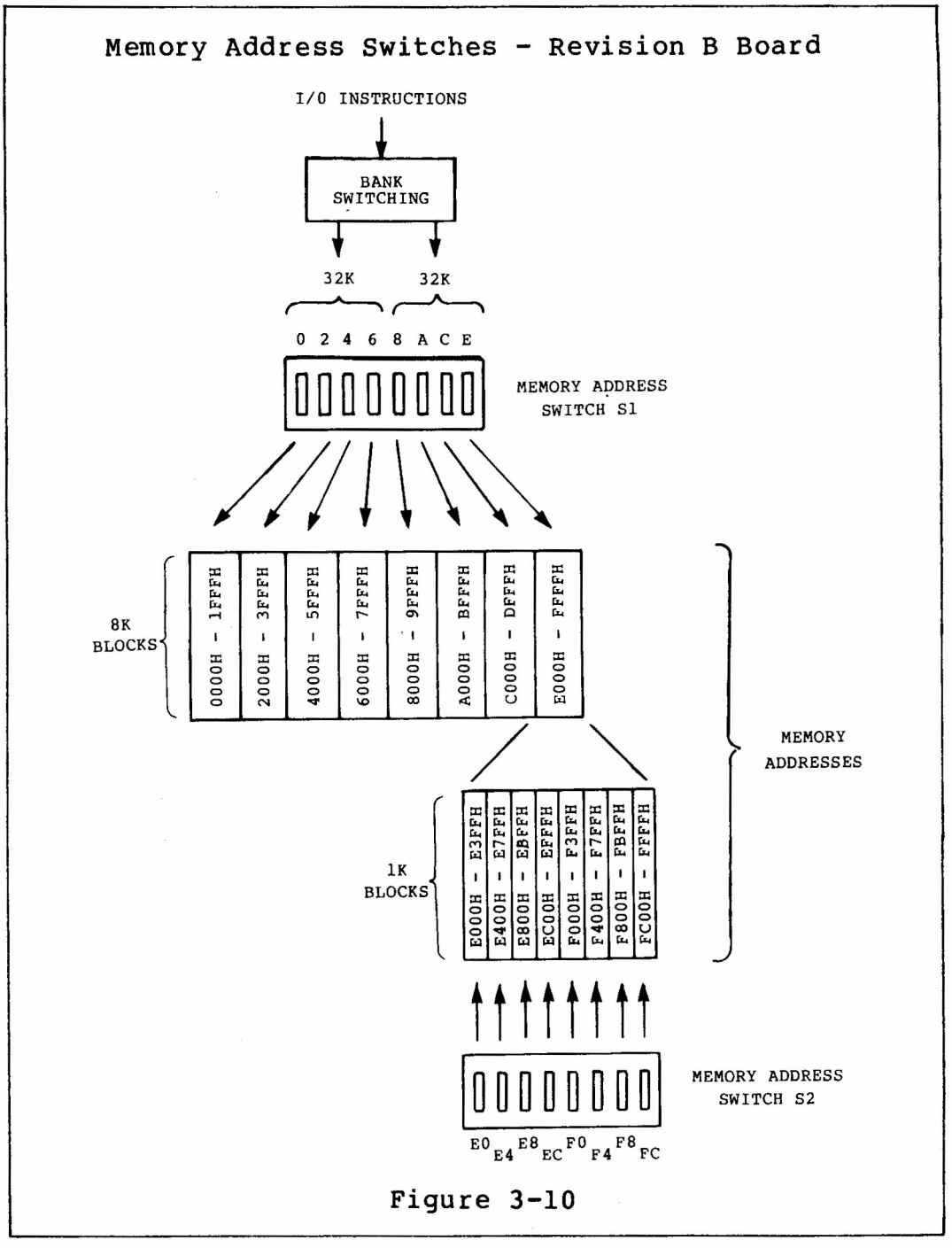


Figure 3-10

Each of the switches in S1 corresponds to one 8K section of the address space. The last 8K section is further divided into 1K sections by the switches in S2.

For addresses 0000H through DFFFH, each 8K section is controlled by the switches in S1 and the bank switching scheme described in Section 3.2. In order for any of these 8K sections to be active, the corresponding S1 switch must be on (up), and the corresponding section of the address space must be turned on by the bank switching logic.

The last 8K section, E000H through FFFFH, can either be controlled as described for the other seven sections, or it can be controlled by S2. If it is controlled by S1, then all of the S2 switches must be turned off. If it is controlled by S2, switch E of S1 must be turned off.

If the last 8K section is controlled by S2, individual 1K sections of the address space can be selected, and the selection is independent of bank switching. Any 1K section is selected if the corresponding S2 switch is on, and is not selected if the switch is off. This arrangement allows memory sections E8000H through EBFFH and EC00H through EFFFH to be disabled to allow space for the Disk Controller and Floating Point Board in the Horizon system.

Since the memory selected by S2 is not bank switched, no two banks in the same system may have the same switch in S2 set on. For example, if two banks have switch E0 of S2 turned on, both banks will respond to memory addresses E000H through E3FFH.

3.3.2 Revision E Board

The Memory Address switches allow the HRAM board to respond to some sections of the memory address space and not to others. The correspondence between the Memory Address switches S1 and S2 on the Revision E board and the address space is shown in Figure 3-11.

Memory Address Switches - Revision E Board

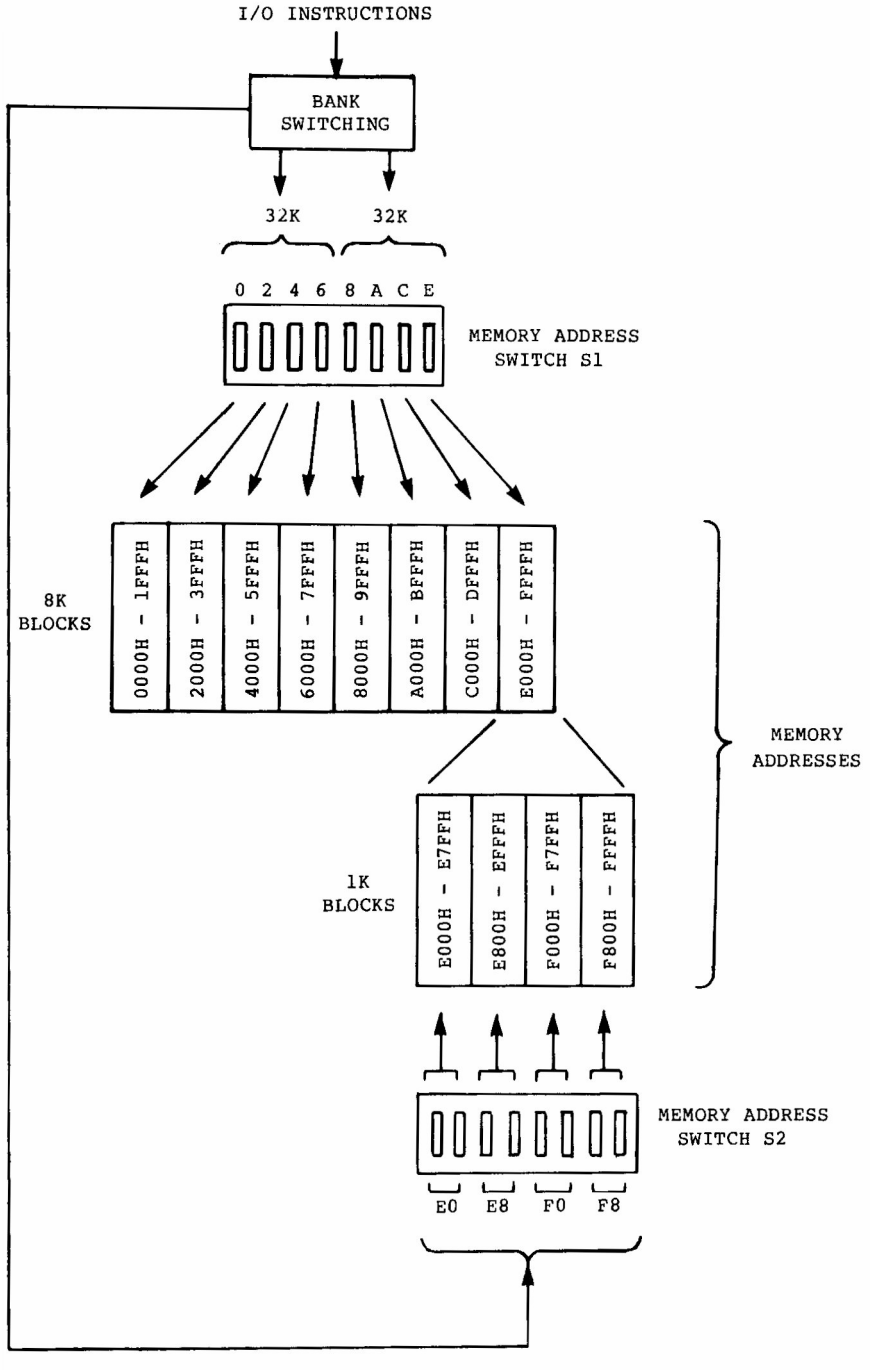


Figure 3-11

Each of the switches in S1 corresponds to one 8K section of the address space. The last 8K section is further divided into 1K sections by the switches in S2.

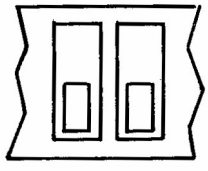
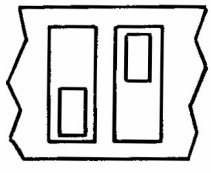
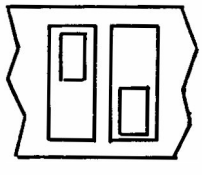
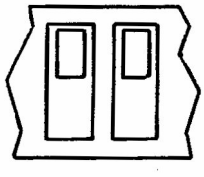
For addresses 0000H through DFFFH, each 8K section is controlled by the switches in S1 and the bank switching scheme described in Section 3.2. In order for any of these 8K sections to be active, the corresponding S1 switch must be on, and the corresponding section of the address space must be turned on by the bank switching logic.

The last 8K section, E000H through FFFFH, can either be controlled as described for the other seven sections, or it can be controlled by S2. If it is controlled by S1, then all of the S2 switches must be turned off. If it is controlled by S2, switch E of S1 must be turned off.

If the last 8K section is controlled by S2, individual 2K sections of the address space can be selected by setting the corresponding pair of switches as shown in Table 3-2. The switch pair can cause the 2K section to be always on, always off, or to be switched on when the bank is switched on. This arrangement allows a 2K memory section to be disabled to allow space for the Disk Controller and Floating Point board in the Horizon system.

Table 3-2

S2 Switch Pairs

Switch Pair in S2	Description
	Corresponding 2K section is always off.
	Corresponding 2K section is on when bank is switched off. This configuration is not normally used.
	Corresponding 2K section is on when bank is switched on.
	Corresponding 2K section is always on.

3.3.3 32K BOARD

If the switches in Memory Address switch S1 are not set properly, the HRAM-32 can respond to more than 32K of address space. For example, if switch 0 and 8 of S1 are both on, the same 8K of memory responds to addresses 0000H through 1FFFH and 8000H through 9FFFH.

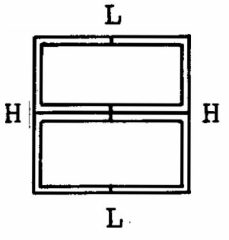
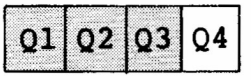
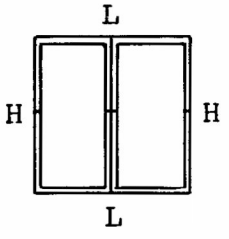
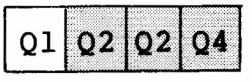
The switches in S1 are normally configured to avoid this double selection by not having both switches in the following switch pairs on at the same time: switches 0 and 8, 2 and A, 4 and C, and 6 and E.

3.4 FIRST QUADRANT OPTION

The First Quadrant option is only available on the revision E HRAM board and is used only with the 48K version of the board. When the option is implemented, it causes the board to respond to the last 48K of the memory address space (4000H through FFFFH) instead of the first 48K (0000H through BFFFH).

This option is implemented by changing the jumper plugs in area JP4. Table 3-3 shows the standard and alternate positions of the jumper plugs in this area and the resulting memory configurations. The shaded blocks in Table 3-3 indicate those quadrants to which the board can respond.

Table 3-3
The First Quadrant Option

Jumper Area JP4	48K Memory Configuration
 STANDARD	
 ALTERNATE	

3.5 PARITY CHECKING

The parity checking feature makes it possible to detect a memory read or write error and generate a program interrupt if an error occurs.

3.5.1 Designating I/O Port Control Bits

The HRAM uses I/O port C0H to arm and disarm parity error interrupts. A jumper plug in area JP1 determines which of three possible bits of the output byte will be used to arm or disarm parity error interrupts from the memory board to the processor.

The HRAM is shipped with the jumper plug positioned as shown in Figure 3-12. This selects bit 6 as the control bit and is the North Star standard configuration. Bits 5 or 7 may be selected by connecting pin P to to pins 5 or 7 respectively (see Figure 3-5).

JP1 Selecting I/O Control Bit 6

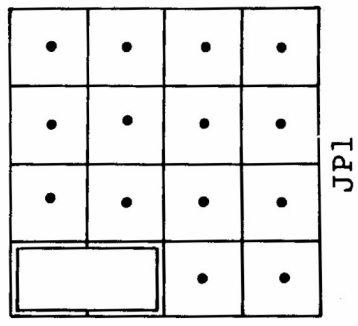


Figure 3-12

3.5.2 Designating Parity Error Response

When the parity logic is armed and an error occurs, one of ten possible interrupts can be generated. The position of the mini-jump in JP3 allows the user to select one of eight vectored interrupts (VI0 - VI7), one nonvectored interrupt (PINT), or one non-maskable interrupt (NMI). As shipped, the board is jumpered to select VI5 as shown in Figure 3-13. This is the North Star standard required by DOS and other operating systems.

JP3 Selecting Vectored Interrupt 5

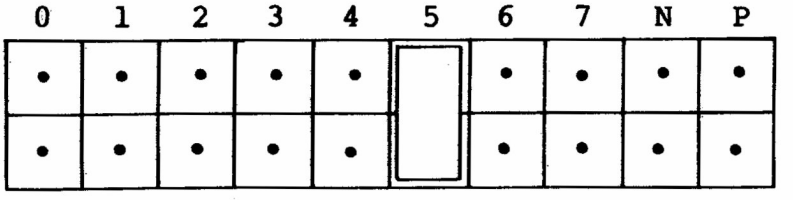


Figure 3-13

If you are using other software, you can pick another interrupt. NMI should only be used as an emergency service technique. If no interrupt is desired, the mini-jump can be stored by placing it sideways, as shown below.

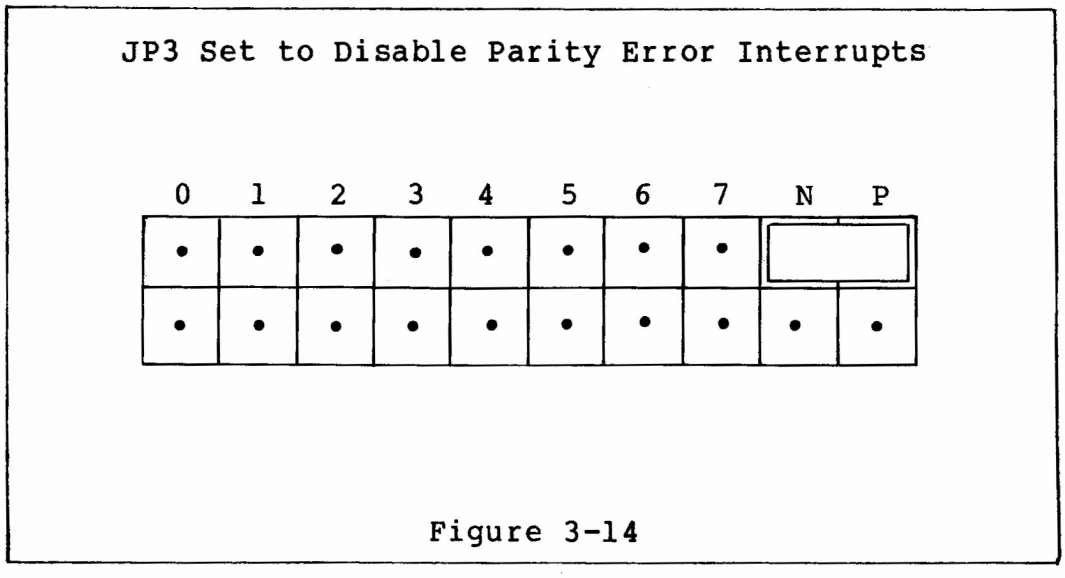


Figure 3-14

3.5.3 Software Instructions

The following instructions indicate how to arm and disarm parity checking. This example assumes that bit 6 has been selected.

```
MVI A,41H    ; Clear any previous parity errors and
OUT 0C0H     ; arm parity interrupts

MVI A,40H    ; Clear any previous parity errors and
OUT 0C0H     ; disarm parity interrupts
```

Note that bit 0 is used to specify turning the condition on or off. If you choose a different I/O bit, change the program instructions accordingly. If you move the mini-jump in JP1 to select bit 5 instead of bit 6, the operands should change from 41H and 40H to 21H and 20H. If you select bit 7, the operands should change from 41H and 40H to 81H and 80H.

3.6 BOARD AND SCHEMATIC REVISION LEVELS

To determine the revision level of the HRAM board, look on the board for jumper area JP4 shown in Figure 3-2. Revision E boards have this jumper area but revision B boards do not.

The revision A schematic corresponds to the revision B board and the revision C schematic corresponds to the revision D board.

It is always advisable to test the HRAM board before actually using it.

To test the HRAM, install it in a HORIZON system and run the RAMTEST3 or RAMTEST5 diagnostic programs. These programs are on the DOS 5.2 diskette. They are described in the System Software Manual Addendum, dated July 1980.

Figure 5-1 shows a block diagram of the HRAM board. The blocks in this diagram are coordinated with the schematics in Appendix D. Each block corresponds to a shaded area of the schematics. In addition, the names used in the blocks are the same as those used in the schematics.

5.1 OVERVIEW

Data from the processor is written into the memory via the 8-bit Data Output (DO) bus. Input buffers isolate all eight signals. The parity generator computes the parity of each 8-bit byte, and adds a ninth parity bit. Each of these 9-bit bytes is then stored in one of the blocks of RAM chips/ The HRAM uses odd parity.

The design of the HRAM is based on the 16K x 1 dynamic RAM chip known as the 4116. These chips are arranged in rows to form 16K 9-bit bytes. The HRAM-64 contains four rows of RAM chips, the HRAM-48 has three rows, and the HRAM-32 has two rows. Since each byte includes a ninth bit for parity error checking, the HRAM-64 contains 36 RAM chips in all; the 48K version has 27 chips, and the 32K has 18 chips.

As data is read out of the memory, the parity checker examines the parity of the byte to insure that it is odd. The data is then transferred into output latches. These latches hold the data stable while it is sent back to the processor on the Data Input (DI) bus.

HRAM Block Diagram

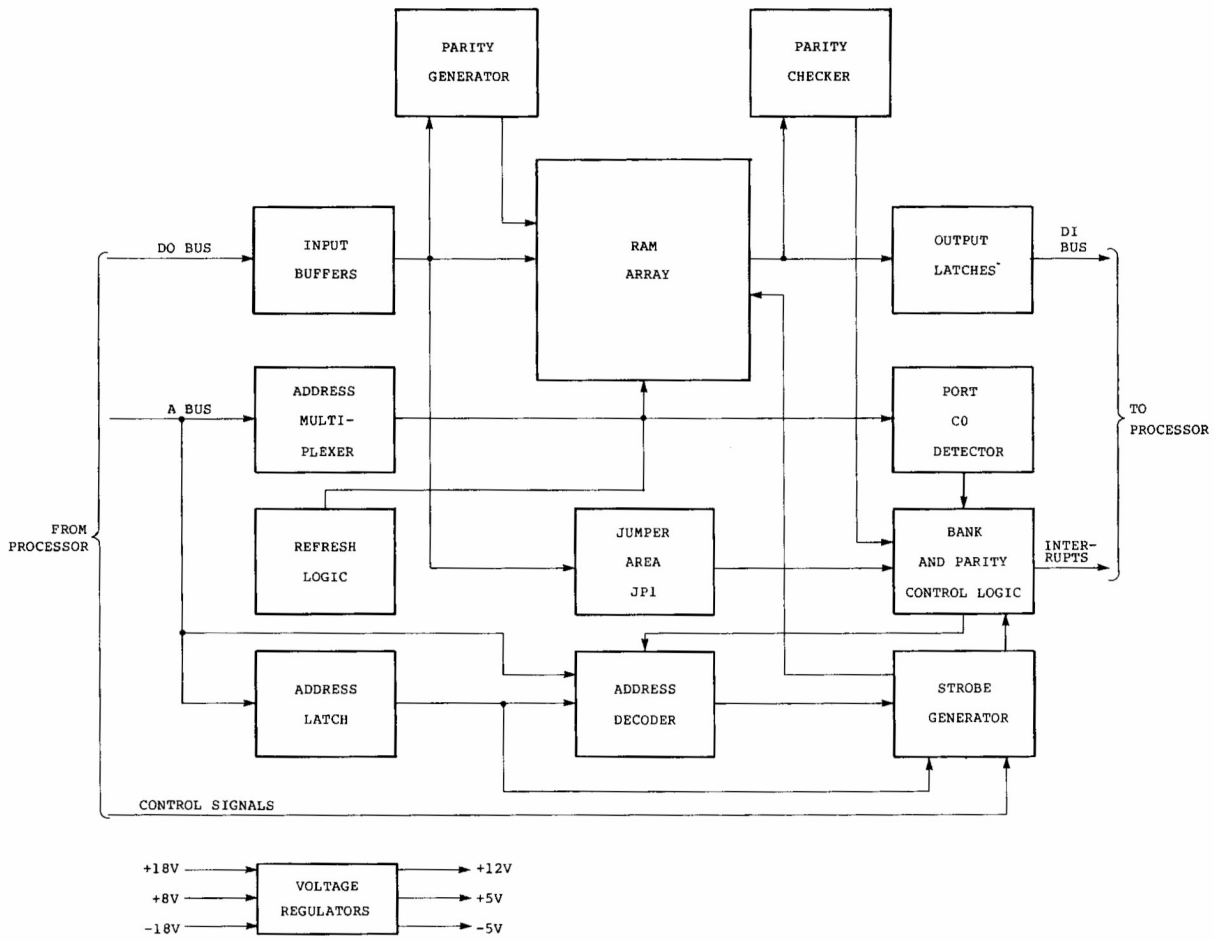


Figure 5-1

The 16-bit memory address enters the board on the A Bus and is used by the HRAM in the following ways:

1. The four most significant bits are used by the Address Latches and decoders to determine if this board should respond to the memory address.

2. The two most significant bits are used by the Cycle Control and Strobe Generator to determine which of the four rows of RAM chips should respond.

3. The least significant 14 bits are used by the RAM array to determine the address inside the selected RAM chips.

4. The least significant eight bits are used by the Port C0 Detector to determine when an output instruction is directed to the HRAM board.

5.2 ADDRESS MULTIPLEXER

The Address Multiplexer receives memory address bits A0 through A13 and sends these bits to the Memory Array 7 bits at a time. Bits A0 through A6 become the row address for the RAM chips and bits A7 through A13 become the column address.

5.3 REFRESH LOGIC

The Refresh Logic supplies the RAM array with a 7-bit address on each memory refresh cycle. The address determines which row of cells in the RAM chips is to be refreshed on that particular refresh cycle. The address automatically increments so that a different address is presented on each refresh cycle.

The host system must generate at least 128 refresh cycles in any 2 millisecond period. Because of this requirement, the memory contents may be jeopardized by a single long wait state on the order of 2 milliseconds, or a series of short wait states.

The Z80 initiates one refresh cycle after each instruction read cycle. Block move instructions provide two refresh cycles per byte moved.

5.4 PORT C0 DETECTOR

The Port C0 Detector examines the low order eight bits of the memory address (A0 through A7) and brings signal $\overline{\text{PORT MATCH}}$ to a slow level when these bits contain a hexadecimal C0. $\overline{\text{PORT MATCH}}$ is used to determine when an output instruction is being issued to the HRAM board.

5.5 ADDRESS LATCH

The Address Latch stores the upper four bits of the memory address (A12 through A15) whenever the Central Processor accesses memory. These bits are used by the Address Decoders and by the Strobe Generator.

5.6 ADDRESS DECODER

The Address Decoder determines whether this HRAM board will respond to the current memory access.

In a revision B HRAM board, the Address Decoder examines the upper six bits of the memory address, the $\overline{E0}$ and $\overline{E8}$ signals from the Parity and Bank Switching Logic and the setting of the Memory Address switches S1 and S2. Signal $\overline{E0}$ is low when the HRAM board is allowed to respond to addresses in the range 0000H through 7FFFH. Signal $\overline{E8}$ performs the same function for the address range 8000H through FFFFH.

The Address Decoder sets the SEL signal high if the memory address is within a bank that is switched on and the corresponding switch in S1 or S2 is turned on. Memory Address switches are described in Section 3.3.

In a revision D HRAM board, memory address bit A10 is removed from the Address Decoder input and the OCCLUDE signal is added in its place. The OCCLUDE signal is high whenever the memory bank on this HRAM board is switched off.

The addition of the OCCLUDE signal causes the following changes in the operation of Memory Address switch S2:

1. The switches in S2 operate in pairs rather than singly.

2. Each switch pair can cause its associated memory address space to be always on, always off or switched along with the memory bank.

5.7 JUMPER AREA JP1

This jumper area is used to select the following options on the HRAM Board:

1. It determines the status of the memory bank on this HRAM Board when the $\overline{RWR}$ signal in low (see Section 3.2.4). $\overline{RWR}$ is generated by the Power on Clear (POC) signal.

2. It determines the output byte that the program must use when setting and resetting the memory bank on the HRAM board (see Section 3.2.2 and 3.2.3).

3. It determines the output byte that the program must use when arming and disarming the parity error checking (see Section 3.5.1 and 3.5.3).

5.8 BANK AND PARITY CONTROL LOGIC

The Bank and Parity Control Logic performs the following functions:

1. It responds to program commands to switch the memory bank in the HRAM board on and off (see Section 3.2.2 and 3.2.3). The resulting OCCLUDE signal is high when the bank is switched off and low when the bank is switched on.

2. It determines how much of the memory will be bank switched. The jumper plugs in jumper area JP2 make this determination (see Section 3.2.1).

3. It responds to program commands to arm and disarm the parity error interrupt feature (see Sections 3.5.1 and 3.5.3). The resulting PARITY ARM signal is high when the feature is on and low when the feature is off.

4. It determines when a parity error has occurred on the HRAM board. Signal PARITY ERROR is set high to indicate the error.

5. It determines which interrupt to generate in response to a parity error (see Section 3.5.2). The jumper plug in area JP3 makes this determination by connecting the PARITY INT signal to one of10 interrupt lines: $\overline{V10}$ THROUGH $\overline{V17}$, $\overline{NMI}$ and $\overline{PINT}$.

5.9 STROBE GENERATOR

The Strobe Generator produces various strobes and timing pulses used throughout the HRAM board. It also selects one of the four possible rows of RAM chips each time the RAM array is accessed.

The basic timing for the Strobe Generator is produced by a 5-stage delay module which is triggered when the START signal goes high. The timing of the module output signals is shown in Figure 5-2.

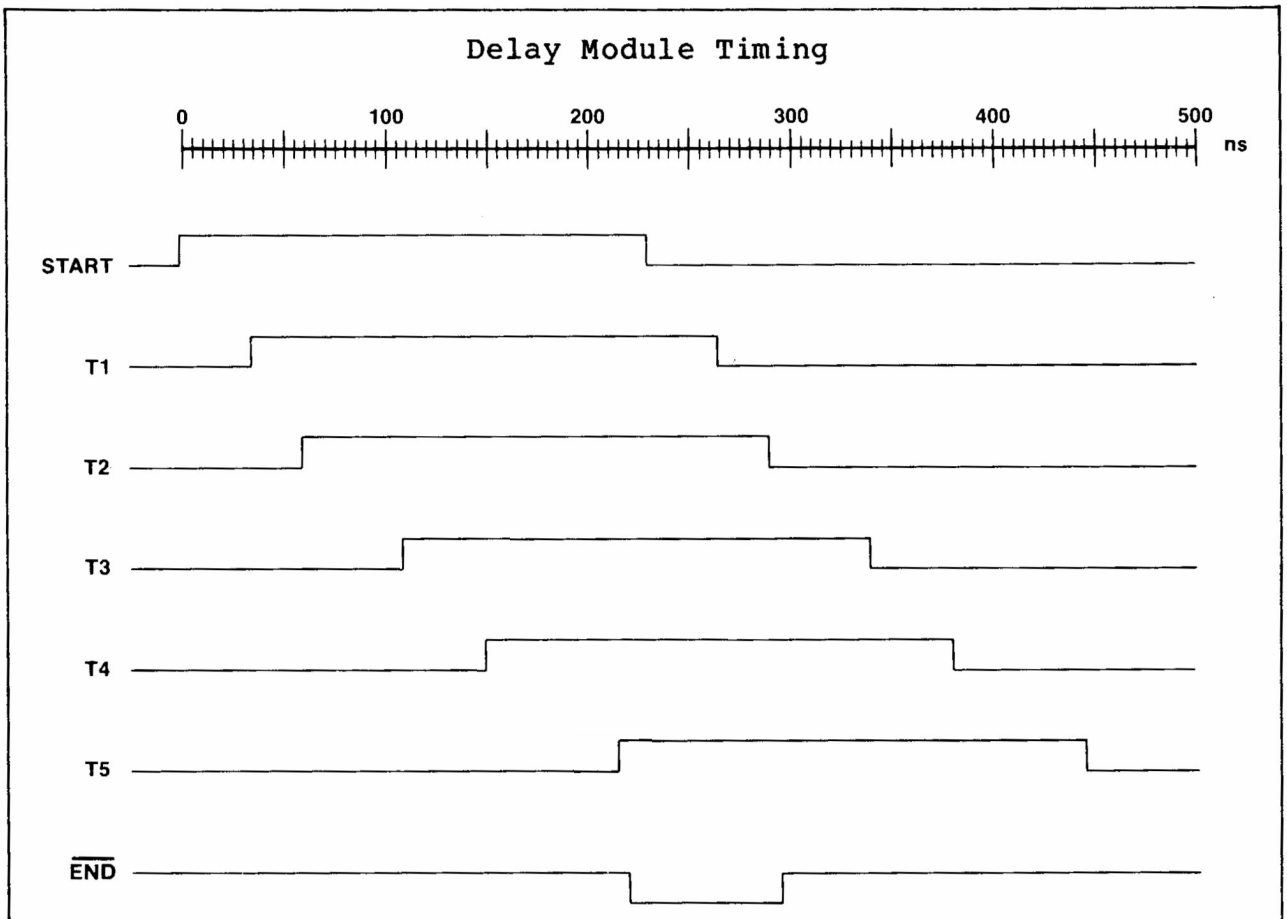


Figure 5-2

The Strobe Generator selects one of four rows of RAM chips by generating one of four row address strobes: $\overline{\text{RAS 1}}$, $\overline{\text{RAS 2}}$, $\overline{\text{RAS 3}}$ or $\overline{\text{RAS 4}}$. The strobe that is generated depends on the memory address, the size of the memory and in some cases, on whether or not the First Quadrant option is selected (see Section 3-4).

On a revision B 64K or 48K board or on a revision E board of the same size that does not have the First Quadrant option selected, the memory address selects the row address strobes as shown in Table 5-1.

Table 5-1

Chip Selection-64K OR 48K, First Quadrant Option Inactive

Address Range	Row Address Strobe	RAM Chip Locations 64K	48K
0000H - 3FFFH	$\overline{\text{RAS 1}}$	1A-1J	1A-1J
4000H - 7FFFH	$\overline{\text{RAS 2}}$	2A-2J	2A-2J
8000H - BFFFH	$\overline{\text{RAS 3}}$	3A-3J	3A-3J
C000H - FFFFH	$\overline{\text{RAS 4}}$	4A-4J	---

On a revision E 64K or 48K board that does have the First Quadrant option selected, the memory address selects the row address strobes as shown in Table 5-2. The effect of this option is to swap the position of the $\overline{\text{RAS 1}}$ and $\overline{\text{RAS 4}}$ signals and thereby change the RAM chips corresponding to the first and last quadrants of the memory address range.

Table 5-2

Chip Selection-64K or 48K, First Quadrant Option active

Address Range	Row Address Strobe	RAM Chip Locations	
		64K	48K
0000H - 3FFFH	$\overline{\text{RAS 1}}$	4A-4J	---
4000H - 7FFFH	$\overline{\text{RAS 2}}$	2A-2J	2A-2J
8000H - BFFFH	$\overline{\text{RAS 3}}$	3A-3J	3A-3J
C000H - FFFFH	$\overline{\text{RAS 4}}$	1A-1J	1A-1J

On a 32K HRAM, the high order address bit (A15) is not decoded. The result is that both rows of RAM chips on the board ard selected by two ranges of addresses as indicated in Table 5-3. Proper configuration of the Memory Address switches prevents any one memory location from responding to two different addresses. Section 3.3 describes the use of these switches.

Table 5-3

Chip Selection HRAM-32

Address Range	Row Address Strobe	RAM Chip Locations
		32K
0000H - 3FFFH	RAS 1	1A-1J
4000H - 7FFFH	RAS 2	2A-2J
8000H - BFFFH	RAS 1	1A-1J
C000H - FFFFH	RAS 2	2A-2J

5.10 VOLTAGE REGULATORS

There are three voltage regulators on the HRAM board. These regulators produce +12 volts, +5 volts and -5 volts. All three of these voltages are used by the RAM chips. The +5 volts is also used by the digital logic chips.

All three regulators are linear integrated circuits.

The procedures in the following sections may be used to troubleshoot the HORIZON system when it is suspected that the HRAM board is not functioning properly.

WARNING
DO NOT REMOVE THE COVER FROM THE HORIZON UNTIL THE POWER IS OFF, THE FAN HAS STOPPED, AND THE RED INDICATOR LIGHT ON THE FRONT PANEL HAS FULLY DIMMED. DO NOT TURN THE POWER BACK ON UNTIL THE COVER HAS BEEN REPLACED.
CAUTION
The electronic components on the HRAM board may be damaged by the static electricity which often builds up in the human body. Before touching the memory board, discharge this electricity by touching a grounded metal object, such as the chassis of a Horizon which is plugged into the wall outlet. Follow this procedure each time the board is handled.

6.1 CHECK HRAM SEATING

1. Turn off the HORIZON power.
2. Remove the HRAM and reinstall it, making sure that it is firmly seated in the connector.
3. Turn the power back on, and test the HRAM again.

6.2 CHANGE BOARD SLOTS

1. Turn off the HORIZON power.
2. Move the HRAM to another slot in the card cage and insert the board firmly in the connector.
3. Turn the power back on, and test the HRAM again.

6.3 CHECK HRAM CONFIGURATION

1. Turn off the HORIZON power.
2. Remove the HRAM and recheck the jumper plugs and the Memory Address switches. Chapter 3 describes the use of these components.
3. Reinstall the HRAM.
4. Turn the power back on.
5. If the HRAM configuration was changed in step 2, test the board again. Otherwise, proceed to Section 6.4.

6.4 RUN DIAGNOSTIC PROGRAMS

Load and run the RAMTEST3 or RAMTEST5 diagnostic program. These programs are on the DOS 5.2 diskette. They are described in the System Software Maual Addendum, dated July 1980.

6.5 REPLACE HRAM

1. Locate a good, spare HRAM board or another memory board of the same capacity.

2. Turn off the HORIZON power.

3. Remove the HRAM.

4. Check the configuration of the spare memory board to insure that it will respond to the desired range of addresses.

5. Install the spare memory board in the card cage and insert it firmly in the connector.

6. Turn the power back on, and test the system with the spare board installed.

6.6 REPAIR PROCEDURES

If it is determined that the HRAM board is defective, it can be returned to any North Star Authorized Service Center for repair.

HRAM-64

0000	2000	4000	6000	8000	A000	C000	E000
1J	1J	2J	2J	3J	3J	4J	4J
1H	1H	2H	2H	3H	3H	4H	4H
1G	1G	2G	2G	3G	3G	4G	4G
1F	1F	2F	2F	3F	3F	4F	4F
1E	1E	2E	2E	3E	3E	4E	4E
1D	1D	2D	2D	3D	3D	4D	4D
1C	1C	2C	2C	3C	3C	4C	4C
1B	1B	2B	2B	3B	3B	4B	4B

HRAM-48

0000	2000	4000	6000	8000	A000	C000	F000
1J	1J	2J	2J	3J	3J	-	-
1H	1H	2H	2H	3H	3H	-	-
1G	1G	2G	2G	3G	3G	-	-
1F	1F	2F	2F	3F	3F	-	-
1E	1E	2E	2E	3E	3E	-	-
1D	1D	2D	2D	3D	3D	-	-
1C	1C	2C	2C	3C	3C	-	-
1B	1B	2B	2B	3B	3B	-	-

HRAM-32

0000	2000	4000	6000	8000	A000	C000	F000
1J	1J	2J	2J	1J	1J	2J	2J
1H	1H	2H	2H	1H	1H	2H	2H
1G	1G	2G	2G	1G	1G	2H	2H
1F	1F	2F	2F	1F	1F	2F	2F
1E	1E	2E	2E	1E	1E	2E	2E
1D	1D	2D	2D	1D	1D	2D	2D
1C	1C	2C	2C	1C	1C	2C	2C
1B	1B	2B	2B	2B	2B	2C	2C

NOTE: These charts are valid only if the First Quadrant option is not active (see Section 3.4 and 5.9).

Type of Signal	Signal Name	Description
Address	A15-A0	16 bits of address from the processor
Data	D17-DI0	8 bits of data to the processor
	D07-DO0	8 bits of data from the processor
Cycle Status	SMEMR	True on memory reads
	SOUT	True on output instructions (to ports, not to memory)
	SMI	True on op-code fetches
	$\overline{\text{PRFSH}}$	True on refresh cycles
Strobe	PDBIN	Strobes data to the processor from memory or port
	$\overline{\text{PWR}}$	Strobes data from the processor to memory or port
Interrupt	$\overline{\text{VI0}}$	Vectored interrupt
	$\overline{\text{VI1}}$	"
	$\overline{\text{VI2}}$	"
	$\overline{\text{VI3}}$	"
	$\overline{\text{VI4}}$	"
	$\overline{\text{VI5}}$	"
	$\overline{\text{VI6}}$	"
	$\overline{\text{VI7}}$	"
	$\overline{\text{NMI}}$	Non-maskable interrupt
	$\overline{\text{PINT}}$	Program Interrupt: chiefly for application when vectored interrupts are not used

Type of Signal	Signal Name	Description
Miscellaneous	PHASE 2	Clock from processor-
	$\overline{\text{POC}}$	True when processor is being reset due to power on clear logic or the rear panel reset switch.
	$\overline{\text{PHANTOM}}$	Not used in a standard HORIZON

REVISION B BOARD

ITEM	P/N	QTY	DESCRIPTION	REF
1	00127	1	HRAM PC BOARD	
2	43045	2	IC 74S00 SCHOTTKY	5C,6C
3	43047	2	IC 74S10 SCHOTTKY	5B,7C
4	43048	1	IC 74S20 SCHOTTKY	8C
5	43050	1	IC 74S74 SCHOTTKY	8F
6	43051	1	IC 74S113 SCHOTTKY	8G
7	43001	1	IC 74LS00	5D
8	43004	1	IC 74LSO4	8E
9	43006	1	IC 74LS08	8D
10	43009	1	IC 74LS14	7G
11	43011	1	IC 74LS30	6H
12	43016	1	IC 74LS75	7D
13	43017	2	IC 74LS109	6D,7E
14	43019	1	IC 74LS132	8K
15	43144	2	IC 74LS156	6B,7B
16	43027	1	IC 74LS161	7F
17	43112	2	IC 74LS244	5G,8J
18	43036	2	IC 74LS258A	5H,6J
19	43040	2	IC 74LS280	5F,6F
20	43043	1	IC 74LS373	6G
21	43044	1	IC 74LS393	8H
22	43066	1	IC 75452	8A
23	43124	36	RAM CHIP/16K X 1/200NS	1A-1J,2A-2J, 3A-3J,4A-4J
			RECOMMENDED TYPES:	
			NATIONAL MM 5290-3	
			MOSTEK MK 4116-3	
			TI TMS 4116-20	
			AMD AM 9016E	
			NEC UPD 416-2	
			MOTOROLA MCM 4116B-20	
24	19002	1	DATA DELAY LINE	1B
25	61014	4	RESISTOR 330 OHM 1/4W,5%	R4-R7
26	61013	1	RESISTOR 220 OHM 1/4W,5%	R1
27	61010	2	RESISTOR 22 OHM 1/4W,5%	R2-R3
28	61086	1	RESISTOR ZERO OHM	W1
29	61007	1	RESISTOR NETWK 47 OHM 16P, DIP	RN1
30	61001	1	RESISTOR NETWK 22 OHM 16P, DIP	RN4
31	61006	1	RESISTOR NETWK 4.7K (10 POS) SIP	RN3

ITEM	P/N	QTY	DESCRIPTION	REF
32	61003	1	RESISTOR NETWK 2.2K (6 POS) SIP	RN2
33	01041	1	CAPACITOR 22 MF 20V	C3
34	01022	3	CAPACITOR 6.8 MF 35V	C8,C9,C10
35	01021	2	CAPACITOR 2.2 MF 25V	C1,C2
36	01002	4	CAPACITOR 47 PF	C4-C7
37	01001	61	CAPACITOR .047 MF CER	BY-PASS
38	65002	1	VOLTAGE REGULATOR 7805	VR1
39	65003	1	VOLTAGE REGULATOR 79L05	VR2
40	65006	1	VOLTAGE REGULATOR 79L05	VR3
41	68006	2	SWITCH 8 POS	S1,S2
42	22001	1	LED - RED	DE1
43	13028	36	SOCKET 16 PIN	1A-1J,2A-2J, 3A-3J,4A-4J
44	13030	1	SOCKET 20 PIN	6G
45	38042	1	HEATSINK 6106	VR3
46	38043	1	HEATSINK 6107	VR2
47	38011	2	HEX-NUT 6-32X1/4 AF MS	
48	38018	2	SCREW,MACH,PH,6-32X3/8	
49	38002	2	LOCKWASHER #6	
50	1309303	1	HEADER,DOUBLE ROW 3 PIN	JP2
51	1309304	2	HEADER,DOUBLE ROW 4 PIN	JP1
52	1309310	1	HEADER,DOUBLE ROW 10 PIN	JP3
53	13087	6	MINI JUMPER PLUG	JP1(3EA) JP2(2EA) JP3(3EA)

REVISION E BOARD

ITEM	P/N	QTY	DESCRIPTION	REF
1	00127	1	64K RAM FAB	D00127
2	43045	2	IC 74S00 SCHOTTKY	5C,6C
3	43047	2	IC 74S10 SCHOTTKY	5B,7C
4	43048	1	IC 74S20 SCHOTTKY	8C
5	43050	1	IC 74S74 SCHOTTKY	8F
6	43051	1	IC 74S113 SCHOTTKY	8G
14	43001	1	IC 74S500	5D
15	43004	1	IC 74S504	8E
16	43006	1	IC 74S508	8D
17	43009	1	IC 74S514	7G
18	43001	1	IC 74S530	6H
19	43016	1	IC 74S575	7D
20	43017	2	IC 74S5109	6D,7E
21	43019	1	IC 74S5132	8K
22	43144	2	IC 74S5156	6B,7B
23	43027	1	IC 74S5161	7F
24	43112	2	IC 74SS244	5G,8J
25	43036	2	IC 74S5258A	5H,6J
26	43040	2	IC 74S5280	5F,6F
27	43043	1	IC 74S5373	6G
28	43044	1	IC 74S5398	8H
29	43066	1	IC 75452	8A
30	43097	36	RAM CHIP/16K X 1/200NS	1A-1J,2A-2J, 3A-SJ,4A-4J
			RECOMMENDED TYPES:	
			NATIONAL MM 5290-3	
			MOSTEK MK 4116-3	
			TI TMS 4116-20	
			AMD AM 9016E	
			NEC UPD 416-2	
			MOTOROLA MCM 4116B-20	
31				
32	19002	1	DATA DELAY LINE	1B
33				
34				
35	61014	4	RESISTOR 330 OHM 1/4W,5%	R4,R4,R6,R7
36	61013	1	RESISTOR 220 OHM 1.4W,5%	R1
37	61010	2	RESISTOR 22 OHM 1/4W,5%	R2,R3
38	61086	1	RESISTOR ZERO OHM	W1
39	61007	1	RESISTOR NETWORK 47 OHM 16P, DIP	RN1

ITEM	P/N	QTY	DESCRIPTION	REF
40	61001	1	RESISTOR NETWORK 22 OHM 16P, DIP	RN4
41	61006	1	RESISTOR NETWORK 4.7K(10POS) SIP	RN3
42	61003	1	RESISTOR NETWORK 2.2K(6POS) SIP	RN2
43				
44				
45	01041	1	CAPACITOR 22MF 20V	C3
46	01022	3	CAPACITOR 6.8MF 35V	C8,C9,C10
47	01043	2	CAPACITOR 2.2MF 35V	C1,C2
48	01002	4	CAPACITOR 47PF	C4,C5, C6,C7
49	01001	61	CAPACITOR .047MF CER.	BY-PASS
50				
51	65002	1	VOLTAGE REGULATOR 7805	VR3
52	65003	1	VOLTAGE REGULATOR 7812	VR2
53	65006	1	VOLTAGE REGULATOR 79L05	VR1
54				
55	68006	2	SWITCH 8 POS	S1,S2
56				
57				
58	22001	1	DIODE ELECTRO. RED	DE1
59				
60				
61				
62				
63				
64				
65	13028	36	SOCKET 16PIN	1A-1J,2A-2J, 3A-3J,4A-4J
66				
67	13030	1	SOCKET 20PIN	6G
68				
69				
70				
71	38042	1	HEATSINK 6106	VR3
72	38043	1	HEATSINK 6107	VR2
73				
74	38011	2	HEX-NUT 6-32X1/4 AF MS	
75				
76	38018	2	SCREW,MACH,PH,6-32X3/8	
77				
78	38002	2	LOCKWASHER #6	

ITEM	P/N	QTY	DESCRIPTION	REF
79				
80	13093-08	1	HEADER, DOUBLE ROW 3 PIN	JP2
81				
82	13093-04	2	HEADER, DOUBLE ROW 4 PIN	JP1
83				
84	13093-10	1	HEADER, DOUBLE ROW 10 PIN	JP3
85				
86	13087	8	CONN. PCB-"MINI-JUMPER"	JP1(3EA) JP4(2EA) JP2(2EA) JP3(3EA)
87				
88				
89				
90				
91	1309302	1	HEADER, DOUBLE ROW, 2 POS	JP4
92	1309802	1	HEADER, SINGLE ROW, 2 POS	JP6

NOTES

1. Use revision A schematics with an assembly revision B board. This designation is marked on the component side of the board.

2. Use revision C schematics with an assembly revision E board. This designation is marked on the component side of the board.